

The Analysis and Design of Integrated Capacitive Displacement Sensors

by

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Abstract

Capacitive displacement sensors are currently used in high-resolution non-contact displacement measurements such as wafer thickness and flatness. Currently these sensors are fabricated from discrete mechanical and electrical parts, with a triaxial cable connecting the sensor electrode at the mechanical sensor head to the sense electronics on a printed circuit board. By having an integrated front end located in close proximity to the mechanical sensor, we expect to achieve nanometer-order resolution with a precise digital representation of displacement as the output, through elimination of the triaxial cable. This is an improvement over the current sensors in terms of performance and cost. The main tasks of the thesis work are low-noise capacitance measurement circuitry design, high-resolution sigma-delta analog-to-digital converter design based on switched-capacitor techniques, and fabrication of a prototype of the design using a standard CMOS process.

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Chapter 1

Introduction

1.1 Motivation

The rapid evolution of the semiconductor industry, with emphasis on feature size reduction to achieve high performance circuits, demands the development of high precision displacement measurement systems for use in wafer steppers and mask aligners. Such systems are also used in wafer flatness and thickness measurements [1, 2, 3]. Capacitive displacement measurement is frequently used for these measurements because of the inherent contact-less nature of the process. The currently available sensors are fabricated using discrete mechanical and electrical parts. Typically, electronics on a printed circuit board drive a triaxial probe through a triaxial cable. The triaxial electrodes on the probe are sense, guard and ground. The guard electrode is required both to null the cable capacitance and to improve the probe linearity by terminating fringe fields. Figure 1-1 [4] shows an example of such a capacitive displacement probe.

A number of problems are associated with the current approach. First, the assembly process is challenging and expensive. The assembly of the probe triaxial structure must be accurate and be reliably connected to the triaxial cable with no sense/guard

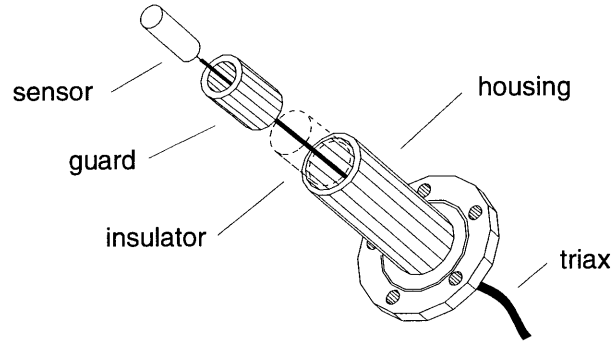


Figure 1-1: Typical capacitive displacement probe (Figure taken from [4])

leakage. The probe sense electrodes must then be precision finished by grinding and lapping to establish a smooth planar surface. Since the sensing electronics is sensitive to femtofarads of capacitance change, the cable must be of a special fabrication to avoid triboelectric charging effects which appear as noise when the cable is moved. The cable is then connected to the sense electronics using a triaxial connector, which is expensive and presents a reliability problem. In addition the cable is a strong source of electrical noise pickup, especially at 60Hz. Finally the fabrication cost is high even in volume production.

By going to an integrated solution, that is, by close integration of the sensor electrodes and the sense electronics, preferably on the same substrate, the above problems can be largely eliminated. A conversion circuit in close proximity to the sensor electrodes can then be used to obtain equivalent digital representations of the sensitive analog measurements. The assembly steps equivalent to those mentioned above, in particular the triaxial cable assembly, probe, and connectors, will be eliminated, leading to lower cost, increased reliability, and increased resolution of capacitive displacement sensing. Such improvements can lead to a much wider range of applications for these sensors.

Examples of similar implementations include the integrated accelerometer widely

employed in the auto industry [5, 6, 7, 8, 9, 10] in which micromachining enables the construction of the sense element together with the electronics required for sensor readout on the same substrate. Similarly the integrated pressure sensor [11, 12] is yet another example. In these examples, sensors and actuators are placed in close proximity with signal processing circuitry leveraging existing integrated circuit manufacturing technology [13]. The most compelling reasons for such an approach is to improve the performance and to lower cost. Often the change in the physical parameter, for instance the capacitance for an integrated accelerometer, is so tiny that it can easily be corrupted by noise introduced by the readout circuitry as well as that coupled via packaging, thus limiting the sensing system resolution. In addition, the increased use of digital signal processing systems dictates a digital sensor output. Consequently an integrated analog-to-digital conversion circuitry [5, 12] based on the sigma-delta approach is favored due to the high resolution, band-limited requirements for the conversion.

1.2 Objective

The objective of this thesis is to investigate the issues involved in the implementation of an integrated capacitive displacement sensor that can satisfy the following specifications:

- digital output as a representation of displacement measured
- displacement range: $100\ \mu\text{m} \pm 50\ \mu\text{m}$
- resolution: 1 part in a million (approximately 20 bits)
- bandwidth: 100Hz minimum

The sensor presented in this thesis shows a promising implementation for an integrated capacitive displacement sensor fabricated using a standard CMOS process.

For the displacement ranges we are considering, the most common sensor currently in use has an active circular sensing area with a diameter of 5 mm. The corresponding capacitance has a range of approximately 1.15 pF to 3.48 pF in air, over the typical measured range of 50 μm to 150 μm . With our target resolution being on the order of 0.1 nm, the change in capacitance to be measured is thus on the order of attofarads.

1.3 Highlights of the Project

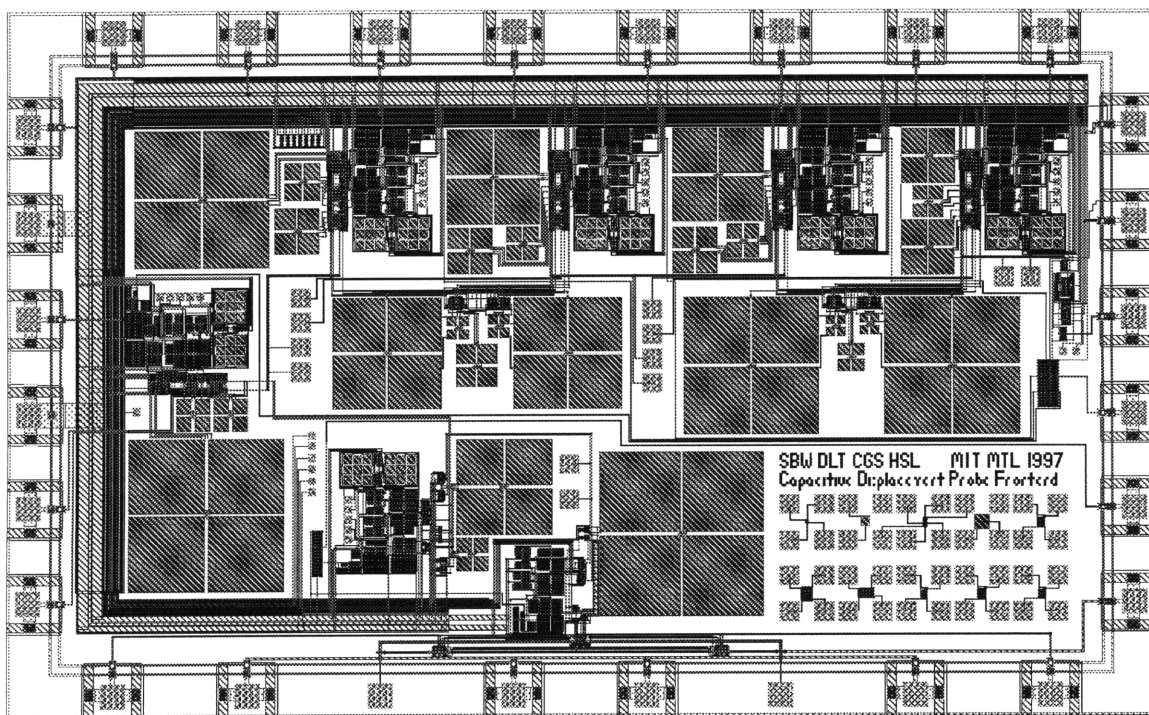


Figure 1-2: Layout of our prototype chip

A prototype test chip was fabricated to demonstrate the feasibility of the integrated capacitive displacement sensor concept. Figure 1-2 shows the layout of the die. In

addition, an analog test board, as shown in figure 1-3, was custom designed for characterization and debug of our prototype chip. The test setup can be seen in figure 1-4. The design of our prototype chip and its associated testing is presented in the later chapters of this thesis.

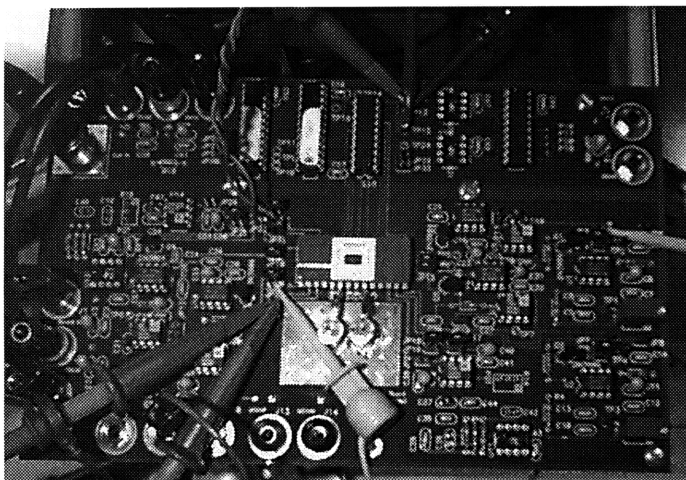


Figure 1-3: Analog test board with prototype chip

1.4 Thesis Organization

Chapter 2 gives an overview of the current implementation of capacitive displacement sensing. The different types of circuitry required to enable a readout of displacement are also presented in this chapter.

The underlying concept of sigma-delta analog-to-digital conversion is presented in Chapter 3. This conversion scheme allows us to achieve high resolution for a limited bandwidth without the use of precision on-chip analog components.

Chapter 4 describes the characteristics of the folded cascode opamp, bias circuit and switched capacitor common mode feedback scheme. This opamp forms the core of our switched-capacitor-based analog-to-digital conversion and is crucial for achieving

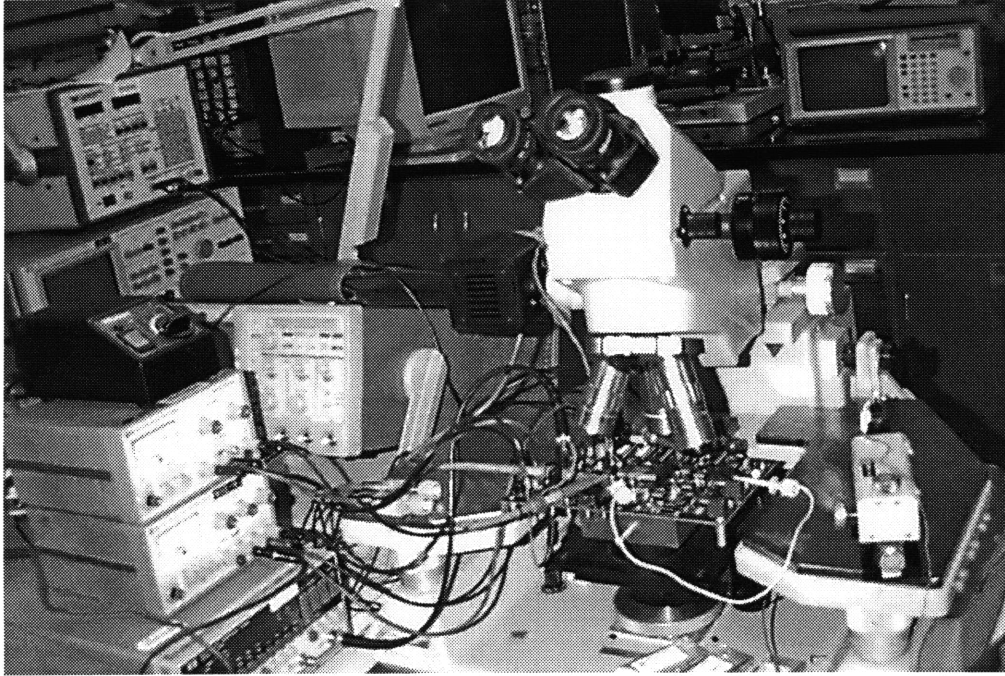


Figure 1-4: Test setup for prototype chip testing and debug

high performance.

The layout of the opamp is shown in chapter 5. Ideas for the incorporation of the capacitance-to-voltage conversion circuitry into the analog-to-digital conversion circuitry and their corresponding implementations are also presented.

Chapter 6 shows test results with our prototype chip. Chapter 7 concludes this thesis with suggestions for future work.

Chapter 2

Capacitive Displacement Sensing

2.1 Introduction

Capacitive displacement measurement systems are currently employed in wafer flatness and thickness measurements [1, 2, 3], where no contact with the target, in this case the silicon wafer, is desired. In addition they also find applications in wafer stepper stages [14] being the fine position sensors for closed loop positioning.

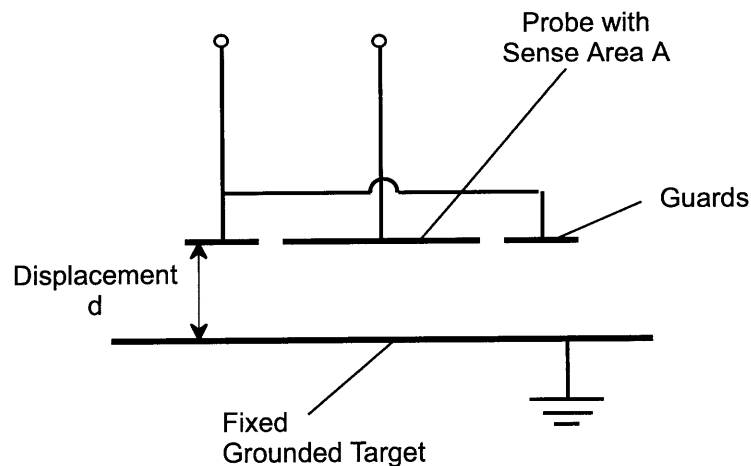


Figure 2-1: Ideal parallel plate capacitor model for displacement sensing

These systems exploit the inverse relationship between the capacitance C and the distance d between the two conducting plates of an ideal parallel plate capacitor with overlapping area A in a medium whose relative permittivity is given by ϵ_r as shown in figure 2-1.

$$C = \frac{\epsilon_r \epsilon_0 A}{d}$$

There are three possible way to change the capacitance of a parallel plate capacitor:

- Variation of the permittivity ϵ_r of the dielectric between the plates [15, 16]
- Variation of the distance d between the plates [17, 18]
- Variation of the area A of overlap between the plates [19, 20, 21, 22]

Here the interest lies in the variation of the distance d . However the same principles for capacitive sensing are also applicable generally to areas where either a capacitance or an inverse of capacitance has to be measured. The ideal relationship holds well for small values of d , provided that one of the plates has an area much larger than the other one, and the smaller plate has guard electrodes driven synchronously with the sensor plate.

Present systems can provide non-contact measurements, while delivering a high resolution, often measured by nanometers. The drawbacks include the constraint to a small displacement range, measured in terms of hundreds of microns, as well as an analog output. The increased use of digital signal processing systems dictates such an analog output be converted to its digital equivalent for data acquisition, storage and analysis. The main difficulty lies with the interface between the sensor and the high-resolution analog-to-digital converter. In the conversion process the sensitive

analog signal is likely to get compromised [14, 23]. It is envisioned that if the analog-to-digital conversion is performed as an integral part of the capacitive sensing process the sensor noise limits should be improved.

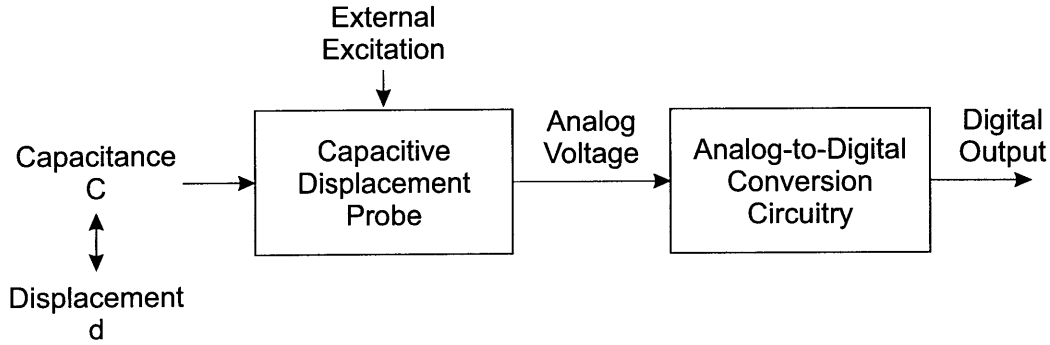


Figure 2-2: Main blocks for capacitance displacement measurement

Hence in order to have a digital representation of the displacement to be measured, the current implementations involve two main components, namely the capacitive-to-voltage conversion circuitry and the analog-to-digital conversion circuitry, as shown in figure 2-2. It is desirable to achieve an integration of these two components for improved overall performance.

2.2 Currently Employed Sensing Schemes

The currently available sensors exploit the $Q = CV$ principle. Here the capacitance C is varied by the distance between the sensor electrode and the grounded target. Numerous techniques exist for measuring small varying capacitances. However not all of them are realizable as an integrated circuit. In addition, a high performance system mandates a minimization of the effect of stray capacitances and a reduction in the baseline drift of the capacitance measurement circuits. A number of these techniques will be reviewed in the following sections.

2.2.1 The Resonance Method

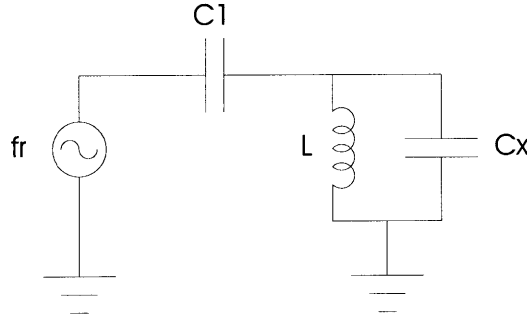


Figure 2-3: Simplified circuit for resonance method

As shown in figure 2-3 [24], the voltage source outputs a sinusoidal signal to a voltage divider formed by a known capacitor C_1 and a LC parallel circuit consisting of a known inductance L and the unknown capacitance C . By adjusting the frequency f_r of the sinusoidal signal, resonance can be found, and the unknown capacitance C can then be calculated:

$$(2\pi f_r)^2 L(C_1 + C) = 1$$

The main limitation is the need to manually adjust the sinusoidal signal frequency until resonance occurs. This is not suitable for monitoring the continuously changing capacitance as in our intended application. In addition the difficulties in the realization of large inductances on an integrated circuit make the method less attractive.

2.2.2 The Oscillation Method

Yet another possibility is to incorporate the sensor capacitance into a network such that the oscillation frequency, or the time it takes to charge and discharge the sensor capacitance back to its original state, changes with the varying capacitance [11, 25, 26, 27, 28, 29, 30, 31, 32, 33]. The cycle time can then be measured using a simple synchronous counter. This is also known as the capacitance-to-frequency conversion

method.

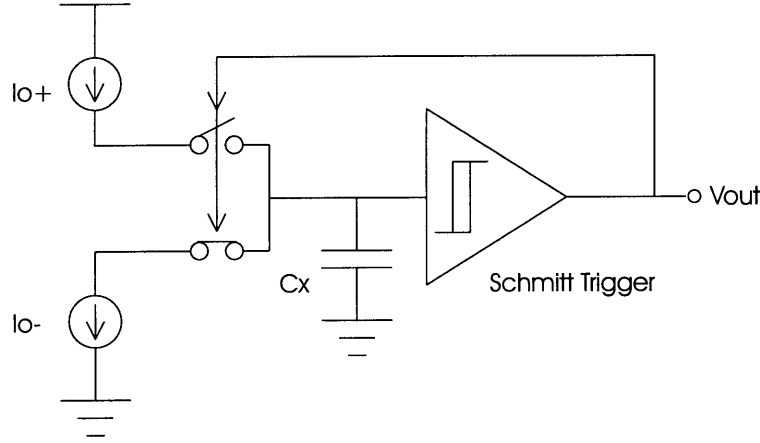


Figure 2-4: Circuit showing capacitance-to-frequency conversion

One possible implementation is shown in figure 2-4. Here C_x is the unknown capacitor and I_{o+} and I_{o-} are constant current sources. The output of the Schmitt trigger determines if C_x is connected to the top or the bottom current source such that it is charged or discharged at a constant rate. As a result the voltage across C_x rises or falls linearly with time. The output voltage V_{out} is a square wave whose period depends on the charging and discharging currents and C_x . Ideally the oscillation frequency is:

$$f_x = \frac{I_o}{2C_x V_h}$$

where V_h is the hysteresis of the Schmitt trigger.

A further improvement is obtained by monitoring the supply currents to the Schmitt Trigger constructed from CMOS circuits, taking note that large currents flow only during transitions. From these current spikes then the oscillation frequency can be measured such that a 2-wire [25, 26] solution is possible.

The main advantage is the ability to be implemented as an integrated form with stray capacitances of lead wires are eliminated. However, this topology offers no

correction for any stray capacitances that appear in parallel to C_x . In addition, at least one complete cycle of charge-discharge is required. This sets a limit on the resolution and the bandwidth of the topology. Given a fixed clock rate for the counter, higher resolution calls for reduced charging and discharging currents and hence longer cycle time and lower resulting bandwidth. Finally the small changes in a relatively large capacitance makes it difficult to obtain high resolution due to the corresponding small changes in the oscillation frequency.

2.2.3 The Charge-Discharge Method

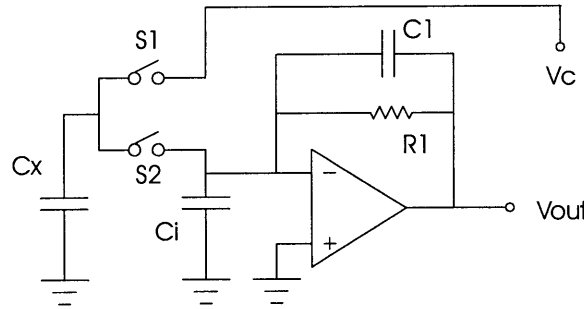


Figure 2-5: Example Circuit for Charge/Discharge

Another possibility would be to charge the unknown capacitor C_x up to a known voltage V_{ref} via a CMOS switch S_1 and then discharge it into a charge detector via a second switch S_2 . This topology is essentially a switched-capacitor based implementation [15, 34, 35, 36].

As shown in figure 2-5, the charge transferred from C_x to the detector in a single charge/discharge cycle is $Q = V_c C_x$. A detector can be implemented such that the charge Q is accumulated on an integrating capacitor C_i for multiple charge/discharge cycles before the voltage across C_i is measured.

A stray insensitive implementation is feasible if both terminals of the unknown capacitor C_x is available. However we have access only to one terminal of our sense

capacitor.

Another switched-capacitor approach uses the charge-balancing concept [37, 38, 39]. In these implementations, the output of a DAC drives the reference capacitor such that the charge on it balances that on the sense capacitor on each charge/discharge cycle. When charge balance occurs, the DAC output is directly proportional to the capacitance C_x to be measured.

One main advantage of this topology is the suitability for integrated circuit design as it is essentially switched-capacitor-based. One drawback is that any stray capacitance in parallel with C_x is indistinguishable from C_x . However, unlike the oscillation topology, the bandwidth is now constrained by the minimum time to charge/discharge C_x fully rather than the cycle time of a synchronous counter.

2.2.4 The Transformer Coupled Charge Pump Method

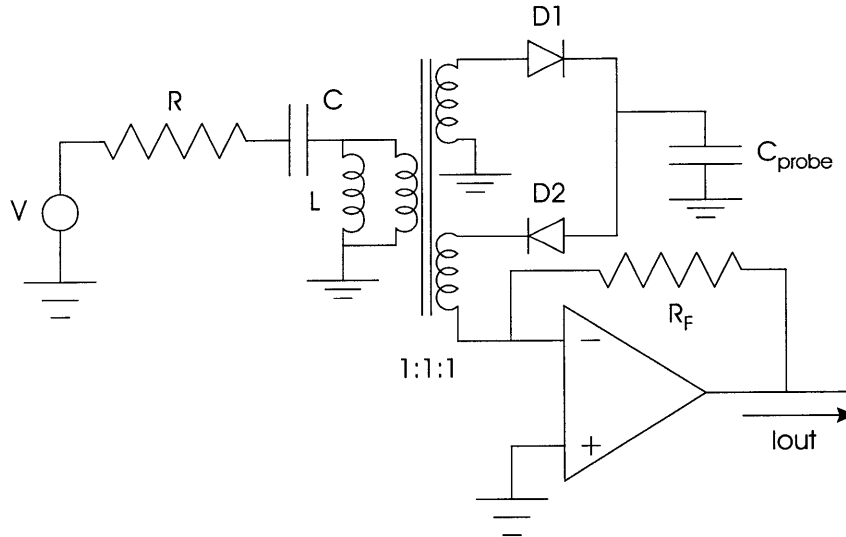


Figure 2-6: Transformer coupled charge pump circuitry

Figure 2-6 shows the transformer coupled charge pump circuit [40]. The inductance L represents the transformer inductance. The voltage source V is a high frequency

source with magnitude V_s . The drive frequency f_s is much greater than $\frac{1}{\sqrt{LC}}$ so that the ac voltage developed across the probe capacitor C_{probe} is essentially the same as the drive voltage, ignoring the diode drops. On each cycle, C_{probe} is charged to V_s through D_1 and then discharged to $-V_s$ through D_2 . Thus an average current I_{out} flows through resistor R_F giving rise to an output voltage.

$$I_{out} = V_s f_s C_{probe}$$

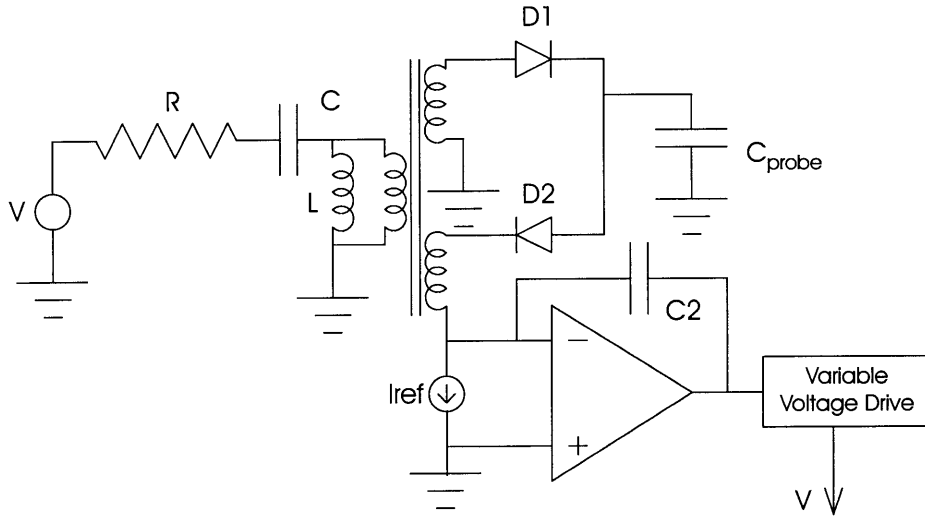


Figure 2-7: Improved transformer coupled charge pump circuitry

An improved version of the transformer coupled charge pump is shown in figure 2-7. By using a variable voltage drive V , the average current flowing out from C_{probe} is forced to assume the value I_{ref} . Now the magnitude V_s of the voltage drive V bears an inverse relationship to the capacitance C_{probe} to be measured.

One main drawback of the design is the use of a transformer that cannot be readily realized as an integrated circuit. An transformer-less implementation [41] based on the charge pump idea is also feasible. However they both suffer from the use of diodes. Although diodes can be easily realized as part of an integrated circuit, the diode drops

are not negligible because the drive voltage is small due to technology limitations.

2.2.5 The Constant Current Method

The inherent advantage of measuring the inverse of capacitances is to have outputs that are directly proportional to the displacements of interest. The inversion is thus performed as an integral part of the design. To do so, one possibility is to transfer a fixed quantity of charge onto the sense capacitor such that the voltage developed is measured. Essentially the average current flowing through the sensor capacitor is kept constant, hence constant current method.

An example of such a design is shown in figure 2-8 [42]. In essence the target and the output of A2 are grounded. The capacitive displacement probe shown has the sense electrode, connected to the inverting input of A2 such that the capacitor formed by the sense electrode and the target is connected across the feedback path of A2. The guard electrodes are connected to the non-inverting input of A2. The high gain of A2 ensures that the guard electrodes are driven to the same potential as the sense electrodes.

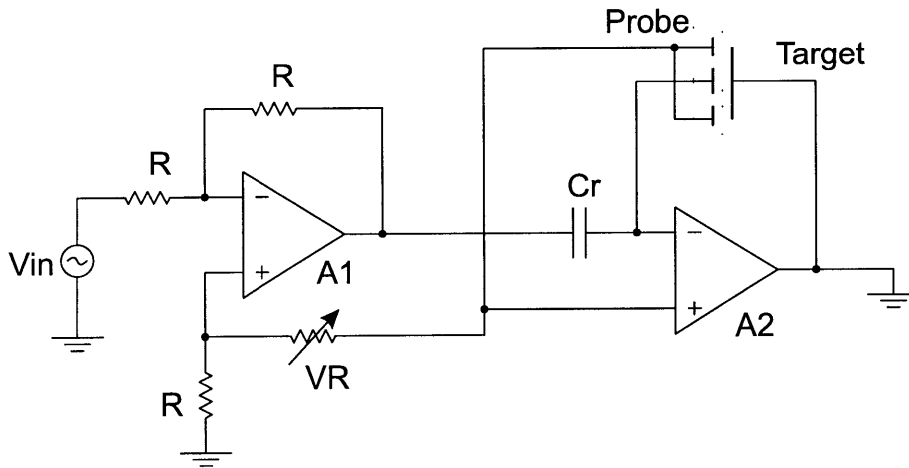


Figure 2-8: $\frac{1}{C}$ Measurement Circuit

Assuming the stray and fringe capacitances is additive to the actual capacitance value measured, the variable resistor VR can be used such that the output voltage, if taken from the non-inverting input of $A2$, is directly proportional to the distance between the grounded target and the sense electrodes of the probe. With the assumption that the amplifiers are ideal, i.e. the positive and negative inputs have the same voltage due to feedback action and no current flows into the amplifier inputs, the following relationships can be derived:

$$V_{outA1} = 2V_{-A1} - V_{in}$$

Resistors R and VR essentially forms a voltage divider such that

$$V_{+A1} = \frac{R}{R + VR} V_{+A2} = \frac{R}{R + VR} V_{out}$$

From charge conservation,

$$(V_{outA1} - V_{out})C_r = V_{out}C_{probe} = V_{out}\frac{\epsilon_0 A}{d}$$

Thus the following relationship between the distance of interest and the output voltage results:

$$V_{out} = \frac{-V_{in}C_r}{\frac{\epsilon_0 A}{d} + C_0 - (2\frac{R}{R+VR} - 1)C_r}$$

where A is the area of the sense electrode, d is the displacement to be measured, C_0 represents stray and fringe capacitances.

Hence an ac analog voltage V_{out} that bears a proportional relationship to the displacement d of interest can be obtained by adjusting the value of VR such that the term $C_0 - (2\frac{R}{R+VR} - 1)C_r$ is set to zero. Demodulation will then enables a dc representation of displacement to be derived.

One main drawback of the design is that the power supplies of both opamps $A1$ and $A2$ have to be referenced with respect to V_{out} taken from the non-inverting input of $A2$. In the current implementation this is achieved with the use of transformer which can not be readily realized as an integrated circuit.

Chapter 3

Sigma-Delta Analog-to-Digital Conversion

3.1 Introduction

The advent of VLSI digital IC technologies has made it attractive to perform many signal processing functions in the digital domain. Oversampled converters are becoming a dominant architecture for high-resolution and band-limited analog-to-digital conversion applications. This technique has been shown to provide high resolution without trimming or high precision components [43, 44, 45].

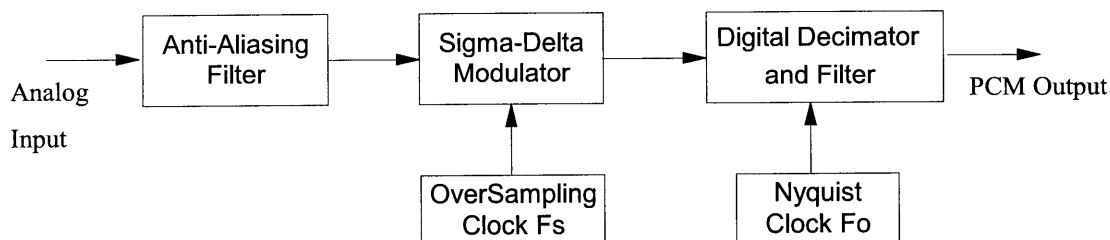


Figure 3-1: Block digram of a typical Sigma-Delta ADC

The class of sigma-delta converters is usually described as oversampling converters.

As shown in figure 3-1, the analog input signal, after passing through an anti-aliasing filter, is oversampled by the modulator at many times the Nyquist rate to produce a coarse quantization. The output is then decimated digitally to give the desired high resolution representation of the original input signal at the Nyquist rate. Quantization noise is effectively moved out of the signal band and can thus be removed by an appropriate digital filter with relative ease.

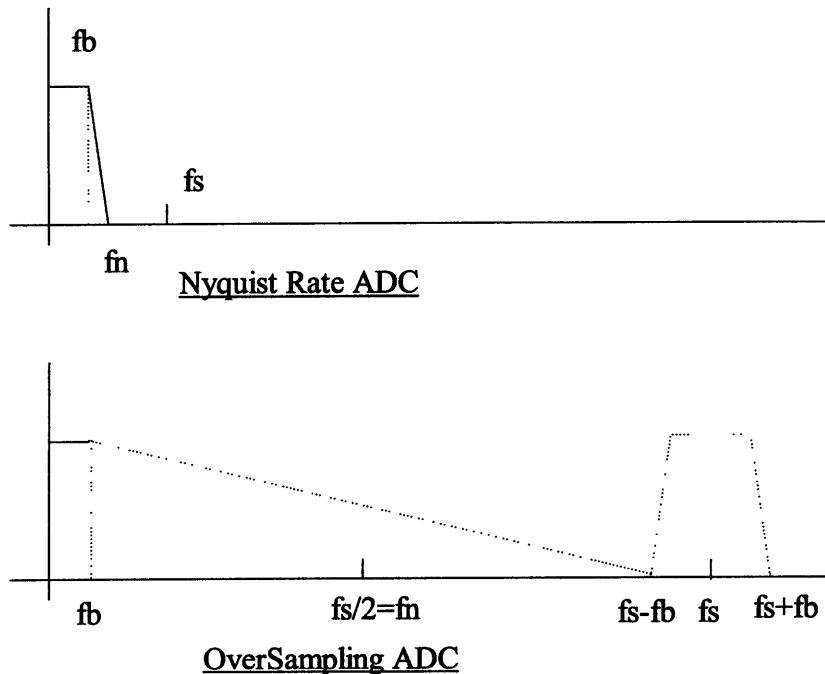


Figure 3-2: Antialias filter requirements for Nyquist and oversample converters

One major advantage of an oversampled A/D system is the reduction in the complexity of the analog circuitry if the encoding is selected such that the modulator needs only to resolve a coarse quantization (usually a single bit). Also, if high oversampling rates are used, the baseband will be a small portion of the sampling frequency. As shown in figure 3-2, with the baseband bandwidth being f_b and the sampling frequency f_s , the analog anti-aliasing filter has a transition band of $f_n - f_b$

in the Nyquist rate converter compared to $f_s - 2f_b$ in the oversampling converter. Clearly the more relaxed constraints permit a more gradual roll-off, linear phase and easy implementation. The precision filtering requirements is now relegated to the digital domain, where a ‘brick-wall’ anti-aliasing filter is required to low pass filter and decimate the digital output down to the Nyquist rate. Additional benefits can be gained with the digital processor which can also be used to provide other functions such as equalization, etc. A system that can provide integrated analog and digital functions and be compatible with digital VLSI technologies is feasible.

In our design, the oversampled sigma-delta modulator forms the core of our implementation that satisfies high-resolution (20-bits) and relatively low-bandwidth (1kHz baseband) requirements. The modulator order, together with a particular noise transfer function, is chosen to meet the analog-to-digital resolution requirement. The implementation is switched-capacitor based and the design is performed in the discrete-time domain based on a linear system model [46, 47]. Simulation was then used for design verification and optimization of filter coefficients. Finally, the modulator was implemented by means of relative scaling of capacitor sizes on silicon. The capacitance-to-voltage conversion is also chosen to be a switched-capacitor based approach that eliminates the need for an anti-aliasing frontend filter.

3.2 Principles of Sigma-Delta Modulators

The simplest form of an oversampled interpolative modulator consists of an integrator, a 1-bit ADC and DAC, and a summer as shown in figure 3-3. The integrator has high gain at low frequencies. Feedback forces the output to lock onto a band-limited analog input. Unless the input exactly equals one of the discrete DAC levels, a tracking error $e(n)$ results. The integrator accumulates this error over time with the DAC output assuming a value that minimize $e(n)$. As a result, the output toggles between the 2

levels such that its average is approximately equal to the average of the analog input.

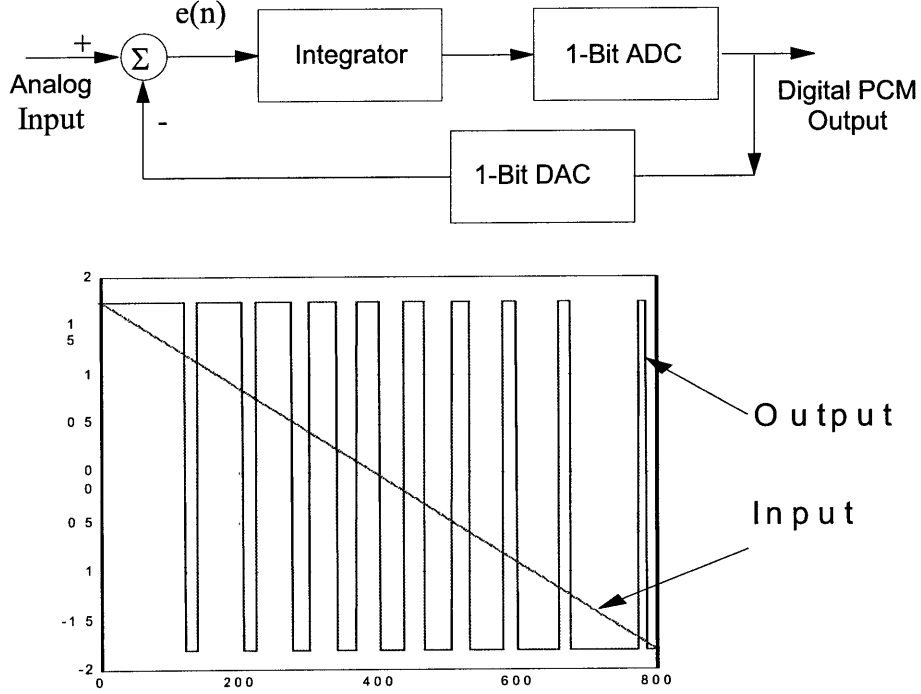


Figure 3-3: First order modulator and its time-domain waveform

The operation of the delta-sigma modulator is analyzed by modeling the integrator with its discrete-time equivalent and the quantization process as an additive noise source $Q(z)$ as shown in figure 3-4. $Q(z)$ is assumed to be a white noise source that is statistically uncorrelated with the input $X(z)$ [43, 48]. Using this linearized model, it can be shown that

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q(z)$$

The overall closed-loop transfer function $Y(z)/Q(z)$ for the quantization noise $Q(z)$ is a high-pass filter whereas that for the input signal $Y(z)/X(z)$ is a pure delay. Hence the *noise shaping* nature of the sigma-delta modulator. From the magnitude

plot of the noise shaping function $|Y(e^{j\omega})/Q(e^{j\omega})| = |1 - e^{-j\omega}|$ as shown in figure 3-5, it is clear that by having the modulator sampling at much higher than the Nyquist rate, quantization noise in the base-band is greatly attenuated. Although a coarse quantization is made by the modulator, most of the quantization noise is pushed to higher frequencies which can then be removed by subsequent digital filtering. Once removed, the final output is a high-resolution digital representation of the input.

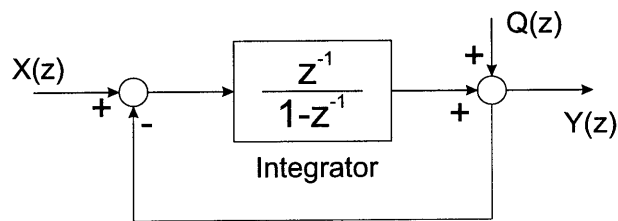


Figure 3-4: Discrete time model of first order modulator

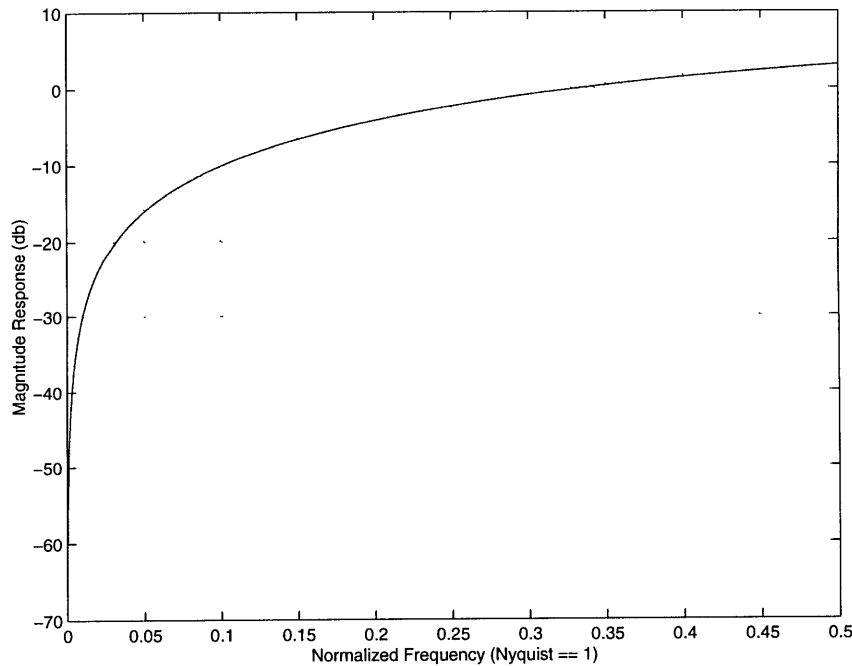


Figure 3-5: Magnitude plot of a first-order noise-shaping function $|1 - e^{-j\omega}|$

The single-bit encoding scheme used has several advantages:

1. The format is compatible for serial data transmission and storage systems. This is important in our implementation since we want to minimize the number of connections between the sensing electronics and the sense electrodes [49].
2. Subsequent digital signal processing operations are greatly simplified as additions and multiplications are reduced to simple logic operations as these operations can be reduced to simple bit-wise operations.
3. The inherent linearity of the in-loop 1-bit DAC guarantees highly linear converters. The integral nonlinearity of the in-loop DAC often limits the harmonic distortion performance of many oversampled A/D converter [50]. A multi-bit DAC has many discrete levels that must be precisely defined to prevent linearity error. With only two discrete values, a one-bit DAC always defines a linear transformation between the analog and digital domains [51]. This guarantees the linearity of the converter.

However many problems arise when implementing a sigma-delta A/D converter. The quantization noise is signal dependent [44, 52, 53] and not statistically uncorrelated as assumed. This is related to the number of state variables in the system. For a sigma-delta modulator, the state of the system is determined by the integrator output value along with the input value. With only one state variable, the loop can lock itself into a mode where the output bit stream repeats itself in a pattern. As a result, the output spectrum can contain substantial peaks centered at multiples of the repetition frequency. To minimize this effect, dithering has been used to randomize the input to avoid the formation of repeating bit patterns. However such a technique lowers the input dynamic range.

By using higher order modulators that involve more than one integrator in the

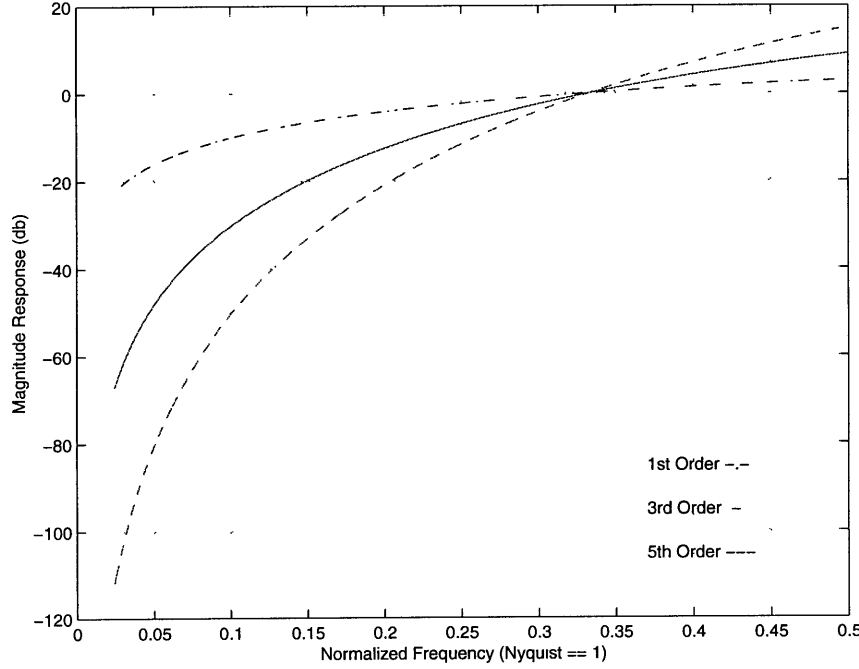


Figure 3-6: Magnitude response for noise-shaping functions of the form $(1 - e^{-j\omega})^N$

loop, repeating bit patterns are less likely to occur, and, consequently, the quantization noise tends to become less signal dependent. In addition, the higher order causes the quantization noise to be further attenuated in the low frequency baseband and to rise more sharply in the higher frequencies, with the net effect being a reduction in the total quantization noise power in the baseband, leading to a higher resolution for the same oversampling ratio. Figure 3-6 shows the magnitude responses of the noise-shaping functions $NS(e^{j\omega}) = (1 - e^{-j\omega})^N$, for $N=1, 3$ and 5 .

Our implementation is based on the single loop 5th order modulator. Single loop higher order modulators are conditionally stable systems, and no exact mathematical analyses exist for such nonlinear systems. In the following sections, the design issues about the order selection, stability analysis and simulation, modulator coefficient selection are presented.

3.3 Order and Noise-Shaping Function Selection

Here the emphasis is on the modulator resolution and bandwidth with power consumption and area being only secondary considerations. Consequently the ideal modulator was designed to resolve better than 20-bit, to account for the inevitable resolution loss once the capacitance measured is inverted to obtain the corresponding displacement values. The modulator design was chosen to give around 140dB signal-to-noise ratio over a baseband of 1kHz.

3.3.1 Design Constraints and Tradeoffs

The design was performed by starting with the noise-shaping function $NS(z)$ of the modulator, assuming a linear additive quantization noise model, as $NS(z)$ will determine the signal-to-noise ratio in the final output. The modulator coefficients can always be derived from $NS(z)$ by algebra. These functions are all discrete-time functions such that it is well-suited for switch-capacitor based implementations. In this phase brick-wall decimation filters, i.e. filters with zero transition region width, are assumed available.

There is as of yet no closed-form solution for the design of stable high-order loops. Instead, the design approach adopted by R. Adams [43, 44, 54] is to ensure that $NS(z)$ exhibit the following properties:

1. $NS(z)$ is a high-pass filter.
2. The high frequency gain of $NS(z)$ is about 1.4.
3. The first value of the impulse response of $NS(z)$ is unity.

The first requirement is a direct result from the need to move the quantization noise out of the low-frequency baseband. The second one comes from the fact that

high frequency gain of $NS(z)$ determines the low-frequency comparator input amplitude, which in turn determines the low-frequency comparator gain as seen by the loop. According to R. Adams [43, 44, 54], such a requirement usually yields a stable first-cut $NS(z)$ whose coefficients are then further adjusted. The loop filter of the modulator has at least one sample delay, as a delay-free loop cannot be easily implemented in the actual switched-capacitor based circuit. Assuming a linear quantizer model, the quantization noise input will then immediately appear at the modulator output. Hence the third requirement results.

The oversampling ratio was chosen to be 512 such that the master clock for the modulator is about 1MHz for a baseband of 1kHz. These were chosen such that the modulator is clocked at a rate that allows full settling of the opamps that make up the design implementation.

$NS(z)$ was chosen to be a 5th order filter. A 4th order $NS(z)$ can just meet the noise shaping requirements. However, the use of a 5th order design allows extra room to account for contributions from other noise sources such as the input referred noise of the amplifiers. In addition, a 5th order design allows using 2 complex zero pairs, producing nulls for quantization noise in the signal passband of the modulator. This leads to further improvements in the signal-to-noise ratio by lowering the quantization noise over a wider range of frequencies compared with a design that places the zeros at DC. As a result, the prototype filter for $NS(z)$ is a 5th order inverse Chebychev filter.

3.3.2 Obtaining Prototype Filter

Using MATLAB, a 5th order inverse Chebychev filter was designed to satisfy the requirements outlined in section 3.3.1. The cutoff frequency w_n and the stopband attenuation R_s were the two variable design parameters. An iterative approach was

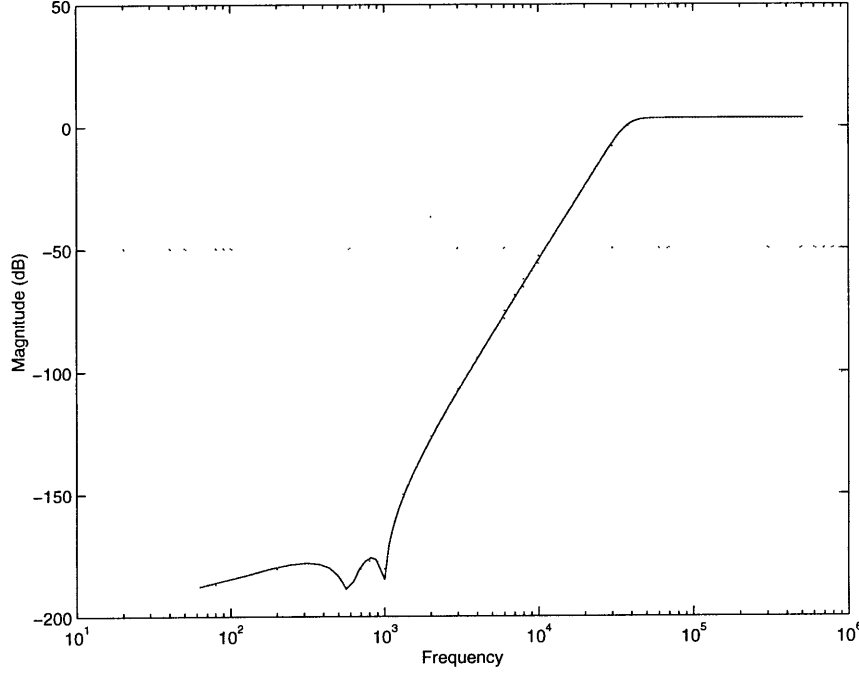


Figure 3-7: Ideal Inverse Chebychev Noise-Shaping Response

taken to determine optimal w_n and R_s . Figure 3-7 shows the frequency response of the resulting $NS(z)$ with $w_n = 0.002$ and $R_s = 180.6$ which meets the design requirements to give an approximate total attenuation of 142.5db for the 1kHz baseband. This translates to approximately 23 bits [55] under ideal conditions.

The zero pairs of the inverse Chebychev filter have frequencies very close to DC such that they are not obvious in the pole-zero plot of figure 3-9. However the nulls they introduced can be easily seen in figure 3-8 which shows the low frequency region of the frequency response.

The resulting $NS(z)$ exhibit the following form:

$$NS(z) = \frac{1 + \alpha_1 z^{-1} + \alpha_2 z^{-2} + \alpha_3 z^{-3} + \alpha_4 z^{-4} + \alpha_5 z^{-5}}{1 + \beta_1 z^{-1} + \beta_2 z^{-2} + \beta_3 z^{-3} + \beta_4 z^{-4} + \beta_5 z^{-5}}$$

with

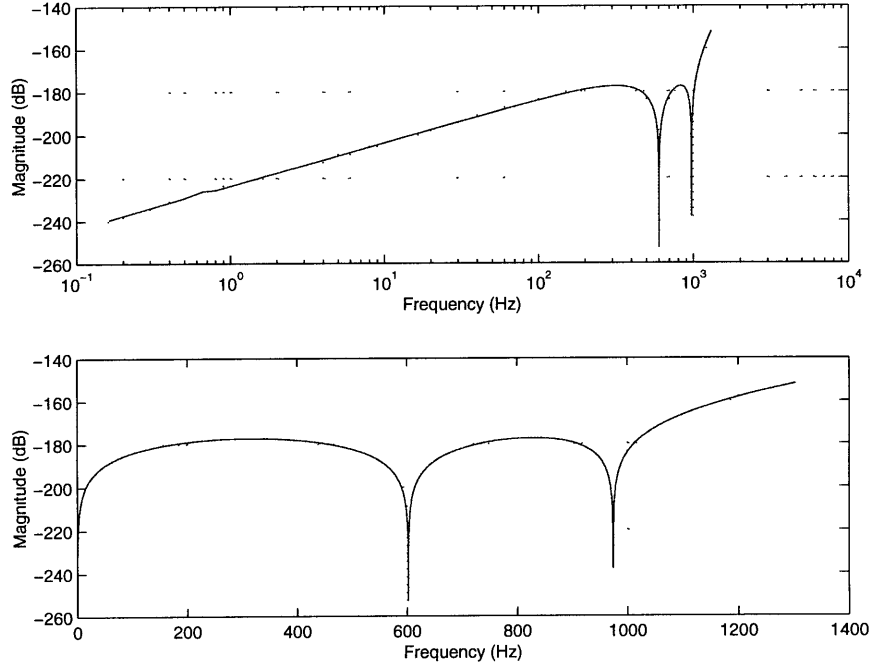


Figure 3-8: Baseband of Ideal Inverse Chebyshev Noise-Shaping Response

α_1	α_2	α_3	α_4	α_5
-4.2567630520	7.2958465820	-6.2888002393	2.7245733959	-0.4744049808
β_1	β_2	β_3	β_4	β_5
-4.9999506520	9.9998519565	-9.9998519565	4.9999506520	-1.0000000000

The incorporation of noise-shaping zeros at frequencies other than DC shifts the β 's slightly. A better appreciation of their presence is the zero and pole locations given below:

Poles:

$$p1 = 0.9096625695 + 0.2024658718i$$

$$p2 = 0.9096625695 - 0.2024658718i$$

$$p3 = 0.8221883699 + 0.1130974371i$$

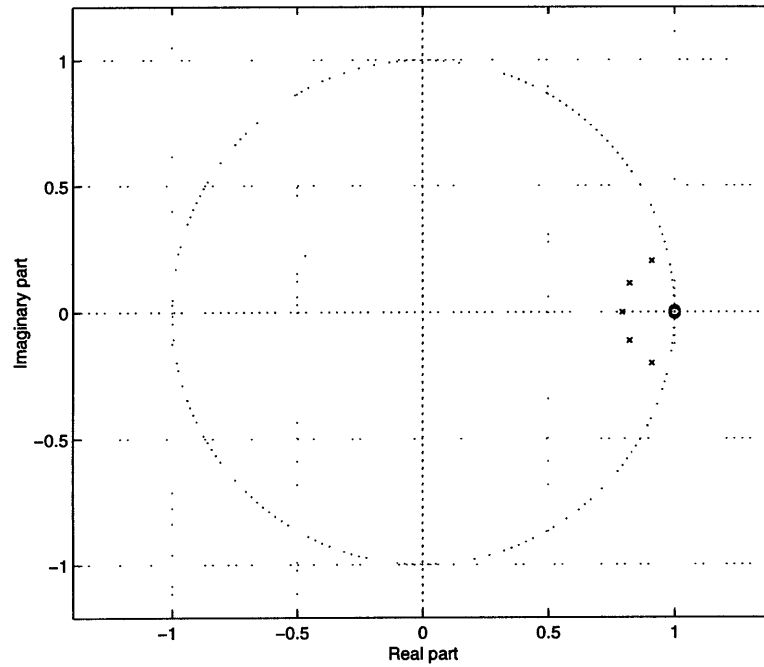


Figure 3-9: Ideal Inverse Chebyshev Filter Pole-Zero Plot

$$p4 = 0.8221883699 - 0.1130974371i$$

$$p5 = 0.7930611733$$

Zeros:

$$z1 = 0.9999827148 + 0.0059756367i$$

$$z2 = 0.9999827148 - 0.0059756367i$$

$$z3 = 1.0000018418$$

$$z4 = 0.9999916903 + 0.0036931540i$$

$$z5 = 0.9999916903 - 0.0036931540i$$

3.4 Coefficient Selection

3.4.1 Derivation of Modulator Transfer Functions

Once the desired noise shaping function is selected, the next step is to determine the coefficients of the linear discrete time modulator model as shown in figure 3-10, i.e. the b 's, c 's and γ 's. The implementation is based on a cascade of 5 integrators with distributed feedback. Two local resonators implement the noise-shaping zero pairs at frequencies other than DC. The distributed feedback nature of the quantized feedback signal in such a realization enhances the stability characteristics even under conditions when one or more of the integrators are in saturation [51].

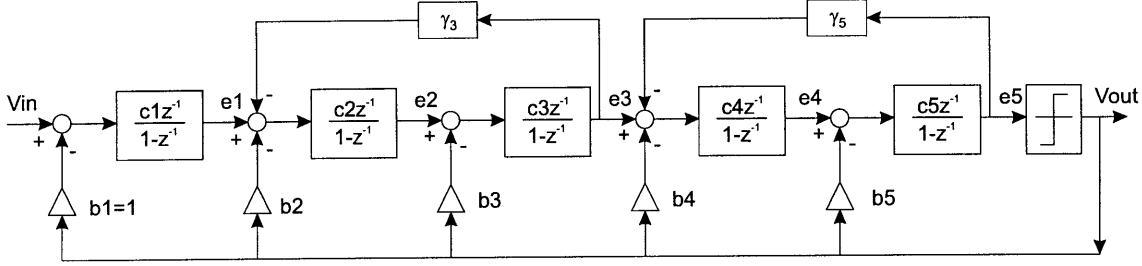


Figure 3-10: Discrete-time model for 5th order modulator

Using a linear model for the quantizer, we can replace the quantizer by a model where the relationship $V_{out} = Q + e_5$ holds [43, 48]. The following equations can then be derived:

$$\begin{aligned}
 e_1 &= \frac{c_1 z^{-1}}{1 - z^{-1}} (V_{in} - b_1 V_{out}) \\
 e_2 &= \frac{c_2 z^{-1}}{1 - z^{-1}} (e_1 - b_2 V_{out} - \gamma_3 e_3) \\
 e_3 &= \frac{c_3 z^{-1}}{1 - z^{-1}} (e_2 - b_3 V_{out}) \\
 e_4 &= \frac{c_4 z^{-1}}{1 - z^{-1}} (e_3 - b_4 V_{out} - \gamma_5 e_5)
 \end{aligned}$$

$$e_5 = \frac{c_5 z^{-1}}{1 - z^{-1}} (e_4 - b_5 V_{out})$$

With these relationships the signal transfer function $\frac{V_{out}}{V_{in}}$ can be found as shown below. It is essentially a low-pass filter function such that signals falling within the baseband can get through the modulator unattenuated.

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{c_1 c_2 c_3 c_4 c_5 z^{-5}}{D(z)}$$

where

$$\begin{aligned} D(z) = & \{(1 - z^{-1})^5 + \gamma_3 c_2 c_3 z^{-2} (1 - z^{-1})^3 + \gamma_5 c_4 c_5 z^{-2} (1 - z^{-1})^3 \\ & + \gamma_3 \gamma_5 c_2 c_3 c_4 c_5 z^{-4} (1 - z^{-1}) + b_3 c_3 c_4 c_5 z^{-3} (1 - z^{-1})^2 \\ & + b_2 c_2 c_3 c_4 c_5 z^{-4} (1 - z^{-1}) + b_1 c_1 c_2 c_3 c_4 c_5 z^{-5} \\ & + b_4 c_4 c_5 z^{-2} (1 - z^{-1})^3 + \gamma_3 c_2 c_3 b_4 c_4 c_5 z^{-4} (1 - z^{-1}) \\ & + c_5 b_5 z^{-1} (1 - z^{-1})^4 + \gamma_3 c_2 c_3 c_5 b_5 z^{-3} (1 - z^{-1})^2\} \end{aligned}$$

Similarly, the noise transfer function $\frac{V_{out}}{Q}$ can be derived. Essentially it is a high-pass filter with large attenuation in the baseband of interest. The width of the baseband, the magnitude of the attenuation and the transition characteristics are the design parameters.

$$\frac{V_{out}(z)}{Q(z)} = \frac{N(z)}{D(z)}$$

where

$$N(z) = (1 - z^{-1})^5 + \gamma_3 c_2 c_3 z^{-2} (1 - z^{-1})^3 + \gamma_5 c_4 c_5 z^{-2} (1 - z^{-1})^3$$

$$+ \gamma_3 \gamma_5 c_2 c_3 c_4 c_5 z^{-4} (1 - z^{-1})$$

Both the noise transfer function and the signal transfer function have the same denominator $D(z)$, a direct consequence of the linear model assumption with V_{in} and Q being the inputs to the loop. $N(z)$ has 4 zeros that are not at $z = 1$ due to the resonators implemented by γ_3 and γ_5 which shift them from DC towards higher frequencies to achieve a improved noise attenuation in the baseband of interest.

3.4.2 Matching Coefficients and Approximations

The more difficult step is to map the coefficients of $NS(z)$ to the ones of the actual modulator implementation comprised of b 's, c 's and γ 's. By choosing the appropriate values for b 's, c 's and γ 's, the swings at the intermediate nodes, namely e_1 to e_5 , will be within the limits defined by the maximum swings of the opamps. The smallest capacitor that can be realized is limited by the parasitic capacitance while the largest capacitor by the area consumption. As a result, the capacitor spread, i.e. the coefficient ratios, has to be minimized.

Here, it becomes a problem of choosing 12 unknowns with only 9 equations. The approach is first to make some approximations to simplify the set of equations and then select certain key modulator coefficients and finally solve algebraically for the rest. Difference equation simulations, using MATLAB and a customized simulator written in C by J. Lloyd [12] extended as part of this thesis project to accommodate resonators used for zero implementation, were used to determine if the constraints on opamp swings and capacitor spreads were met. The procedure involved some trial and error because the problem itself was underconstrained. There can be more than one set of modulator coefficients that implement the same noise transfer function. However only a few sets are feasible due to opamp swings and capacitor spread

limitations.

The 9 equations below relates the modulator coefficients to the numerator and the denominator coefficients for the noise transfer function $NS(z)$:

$$\begin{aligned}
\alpha_2 &= 10 + \gamma_3 c_2 c_3 + \gamma_5 c_4 c_5 \\
\alpha_3 &= -10 - 3\gamma_3 c_2 c_3 - 3\gamma_5 c_4 c_5 \\
\alpha_4 &= 5 + 3\gamma_3 c_2 c_3 + 3\gamma_5 c_4 c_5 + \gamma_3 \gamma_5 c_2 c_3 c_4 c_5 \\
\alpha_5 &= -1 - \gamma_3 c_2 c_3 - \gamma_5 c_4 c_5 - \gamma_3 \gamma_5 c_2 c_3 c_4 c_5 \\
\beta_1 &= -5 + c_5 b_5 \\
\beta_2 &= 10 + \gamma_3 c_2 c_3 + \gamma_5 c_4 c_5 + b_4 c_4 c_5 - 4c_5 b_5 \\
\beta_3 &= -10 - 3\gamma_3 c_2 c_3 - 3\gamma_5 c_4 c_5 + b_3 c_3 c_4 c_5 - 3b_4 c_4 c_5 + 6b_5 c_5 + \gamma_3 c_2 c_3 c_5 b_5 \\
\beta_4 &= 5 + \gamma_3 c_2 c_3 + 3\gamma_5 c_4 c_5 + \gamma_3 \gamma_5 c_2 c_3 c_4 c_5 - 2b_3 c_3 c_4 c_5 + b_2 c_2 c_3 c_4 c_5 + 3b_4 c_4 c_5 \\
&\quad + \gamma_3 c_2 c_3 c_4 c_5 b_4 - 4c_5 b_5 - 2\gamma_3 c_2 c_3 c_5 b_5 \\
\beta_5 &= -1 - \gamma_3 c_2 c_3 - \gamma_5 c_4 c_5 - \gamma_3 \gamma_5 c_2 c_3 c_4 c_5 + b_3 c_3 c_4 c_5 - b_2 c_2 c_3 c_4 c_5 + b_1 c_1 c_2 c_3 c_4 c_5 \\
&\quad - b_4 c_4 c_5 - \gamma_3 c_2 c_3 c_4 c_5 b_4 + c_5 b_5 + \gamma_3 c_2 c_3 c_5 b_5
\end{aligned}$$

where the α 's are the coefficients of the numerator and the β 's are the coefficients of the denominator of the noise transfer function. These were determined as described previously.

The first step to approach the problem is to identify which modulator coefficients can be determined first. From figure 3-10 it can be seen that the choice of c_5 probably does not matter because it is a gain term in front of the non-linear quantization block. Assuming the single-bit quantizer is ideal, changing c_5 does not change the quantizer output. Also, b_1 is chosen to be unity because it is desirable to have V_{out} following V_{in} . Considering the modulator as a feedback loop, the path where b_1 locates is essentially

a negative feedback path such that by setting the gain, i.e. b_1 , to be unity, the error e_1 is minimized and V_{out} tracks V_{in} .

From the α 's, it can be seen that they contain only the following combination of modulator coefficients, namely $c_2c_3\gamma_3$ and $c_4c_5\gamma_5$ such that the zeros of the noise transfer function are the solutions of the following equations in the z -domain:

$$\begin{aligned} (-1 + z) &= 0 \\ (1 - 2z + z^2 + c_2c_3\gamma_3) &= 0 \\ (1 - 2z + z^2 + c_4c_5\gamma_5) &= 0 \end{aligned}$$

By solving for the zero locations, $c_2c_3\gamma_3$ and $c_4c_5\gamma_5$ can be determined. They were found to be on the order of 10^{-5} . An approximation was then made regarding the denominator coefficients i.e. β 's. The terms that involve $c_2c_3\gamma_3$ and $c_4c_5\gamma_5$ were ignored. This simplified the β -related equations greatly as they are now free of γ_3 and γ_5 . Now the denominator coefficients are essentially the same as those of the modulator that does not have resonators which give rise to the γ 's.

The simplified equations relating the modulator coefficients to the denominator coefficients of the noise-shaping function $NS(z)$ are as follows:

$$\begin{aligned} \beta_1 &= -5 + c_5b_5 \\ \beta_2 &= 10 + b_4c_4c_5 - 4c_5b_5 \\ \beta_3 &= -10 + b_3c_3c_4c_5 - 3b_4c_4c_5 + 6b_5c_5 \\ \beta_4 &= 5 - 2b_3c_3c_4c_5 + b_2c_2c_3c_4c_5 + 3b_4c_4c_5 \\ \beta_5 &= -1 + b_3c_3c_4c_5 - b_2c_2c_3c_4c_5 + b_1c_1c_2c_3c_4c_5 - b_4c_4c_5 + c_5b_5 \end{aligned}$$

3.4.3 Optimal Coefficient Selection

The coefficient selection process is a trial-and-error process. With the approximations and preliminary selections made in section 3.4.2, the problem is now reduced to choosing 9 unknowns with 9 equations. However, the difficulty now is that the unknown coefficients are not linearly independent of each other. It seems that these coefficients form pairs such that c_5b_5 has to be determined first, followed by c_4b_4 , c_3b_3 , c_2b_2 and finally c_1b_1 .

The approach is to provide initial guesses of c_1 , b_1 , c_3 , c_4 and c_5 such that corresponding b_2 , c_2 , b_3 , b_4 and b_5 can be derived. Difference equation simulations were then used to check the swings at individual integrator outputs and conditional stability. Simulations were also used to determine how the capacitor spread and the integrator swings are affected by the initial guesses. Based on the trends observed, if any one of the integrator swings becomes too large, another informed guess of the modulator coefficients will be made and the simulation re-run. After some number of iterations, the following modulator coefficients were found:

Coefficient	b_1	b_2	b_3	b_4	b_5
Value	1.0000000	0.6246587	0.4869796	0.4838783	0.2972948
Stable Range	$\pm 5\%$	$\pm 17\%$	$\pm 14.4\%$	$\pm 8.3\%$	$\pm 23.5\%$

Coefficient	c_1	c_2	c_3	c_4	c_5
Value	0.0378000	0.1000000	0.2150000	0.2222000	1.0000000
Stable Range	$\pm 74\%$	$\pm 15\%$	$\pm 9.7\%$	$\pm 22.5\%$	$\pm 98\%$

Coefficient	γ_3	γ_5
Value	0.0006344	0.0000643
Stable Range	$\pm 10\times$	$\pm 10\times$

These modulator coefficients were then implemented as capacitor ratios. The

device-level implementation will be covered in section 5.2.

3.4.4 Numerical Verification

Numerical simulation were used extensively for guiding the modulator design and verification. On the system level, a MATLAB program and the simulator from J. Lloyd were used to independently to numerically verify the implementation and their results cross-checked. For a given sinusoidal input signal, the corresponding modulator spectrum was calculated and the modulator stability verified.

One level down for the implementation is the switched-capacitor based simulation. SWITCAP2 was used for the task. In essence, after the optimal modulator coefficients are determined, they are implemented as capacitor ratios as described in section 5.2. SWITCAP2 then take these capacitor ratios and simulate the whole modulator using ideal switches and amplifiers giving rise to simulation results that are checked against those from numerical simulations.

Figure 3-11 shows a spectrum for the modulator output, using a differential sinusoidal signal of 1kHz at 1.6V peak-to-peak. Numerical accuracy of the simulation makes calculating the signal-to-noise ratio for the implementation difficult. On the other hand, the high frequency noise shaping characteristics match those predicted by numerical simulations and the original prototype filter. This gave a good indication of the correctness of the switched-capacitor implementation.

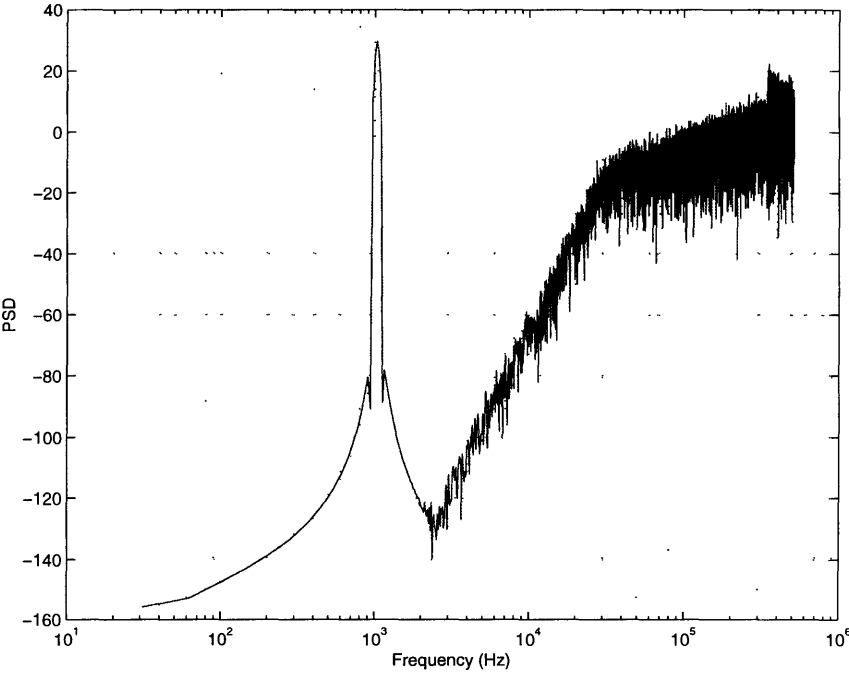


Figure 3-11: SWITCAP2 simulated modulator spectrum

Chapter 4

Operational Amplifier Design

4.1 Introduction

As our implementation is a switched-capacitor based, the most important component is the operational amplifiers (opamps) which form the heart of the design. Two fully-differential designs are used. The only major difference is the implementation of common mode feedback, which is required to ensure the opamp outputs are not saturated.

The performance requirements of the opamps are determined by those of the delta-sigma modulator itself. As the modulator is switched-capacitor based, each individual amplifier has to settle to the desired 20-bit target resolutions of the modulator within half of the period of the clock driving the MOS switches. This means the total settling time is approximately 14 time constants. As the designed clock rate is 1.024MHz, the total settling time is assumed to be half of the period of ϕ_2 plus 20% margin of error. This translates into a time constant τ of:

$$14\tau = 390ns; \tau = 27.8ns$$

If the feedback ratio around the amplifier is β , the relationship between the time constant τ and the unity gain bandwidth f_u can be shown to be:

$$\tau = \frac{1}{2\pi\beta f_u}$$

Assuming a minimum feedback ratio β of $\frac{1}{25}$, we will require the amplifier to exhibit a unity-gain bandwidth of approximately 143 *MHz* in order to meet the 20-bit settling requirement.

The following sections will discuss the fundamentals of the opamp designs, the two different common mode feedback schemes and the reasons behind their usage, and the sizing and biasing of the transistors for gain, settling and noise considerations.

4.2 Folded Cascode Design

Because of the fabrication process chosen, the intrinsic output resistance of the transistors are limited. Cascoding is thus used to boost the overall output resistance. Here a folded-cascode design, essentially a single stage topology, is chosen. An important feature is that the settling behavior is dominated by a single-pole resulting from the amplifier output resistance and the load capacitance. A high phase margin is achievable if only this pole affects the frequency response at crossover. The second pole of this topology arises from the gate and drain capacitances seen at the drains of transistors $M1$, $M2$, $M3$ and $M4$. This second pole prevents a full 90 degrees phase margin to be achieved.

In figure 4-1, PMOS transistors $M1$ and $M2$ form the input differential pair. The use of PMOS input transistors enables NMOS transistors to be used as $M3$ and $M4$. These two transistors carry the largest current and thus have the largest sizes. Being NMOS they can be made approximately 3 times smaller than if they are

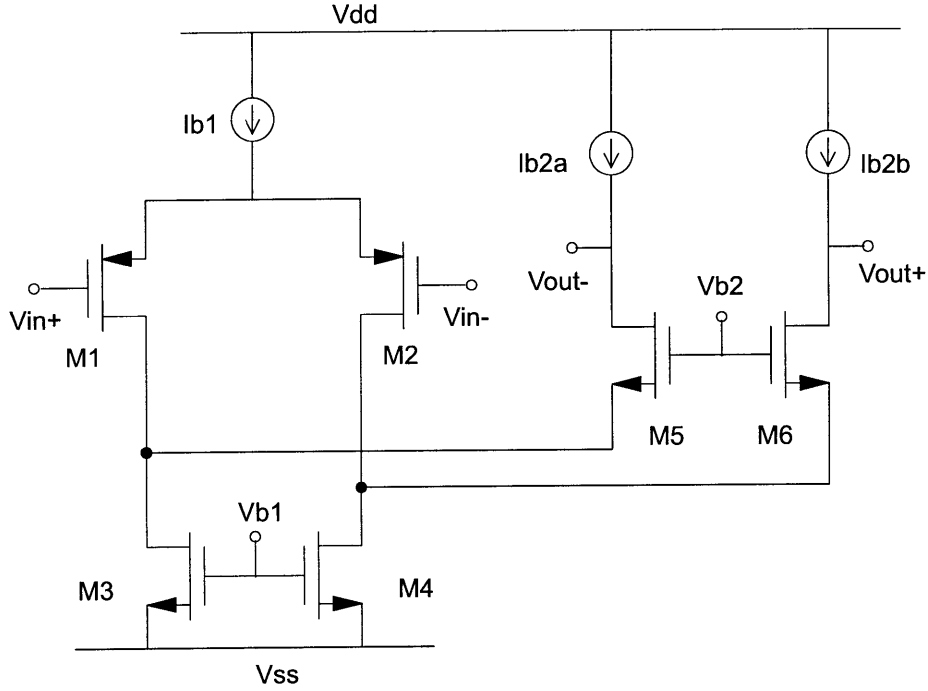


Figure 4-1: Folded cascode opamp design

PMOS, leading to a corresponding smaller capacitance at their drains. Consequently the second pole of the amplifier is high in frequency that the single dominant pole assumption of the design is valid. Transistors $M5$ and $M6$ are the folded cascode transistors. Voltages $Vb1$ and $Vb2$ are fixed bias voltages. The small signal differential voltage gain can be derived by considering only the half-circuit ($M1$, $M3$ and $M5$) as the design is symmetrical.

Figure 4-2 shows the simplified half-circuit schematic used to derive the differential gain. Here the bias current source $Ib2a$ is assumed to be ideal and have finite output resistance R_{op} , which can be derived later from the actual circuit implementation. The source of transistor $M1$ is assumed to be at analog ground for fully differential small-signal input voltages. Hence the output resistance associated with the bias current source $Ib1$ can be safely ignored in the analysis. Being fixed bias voltages,

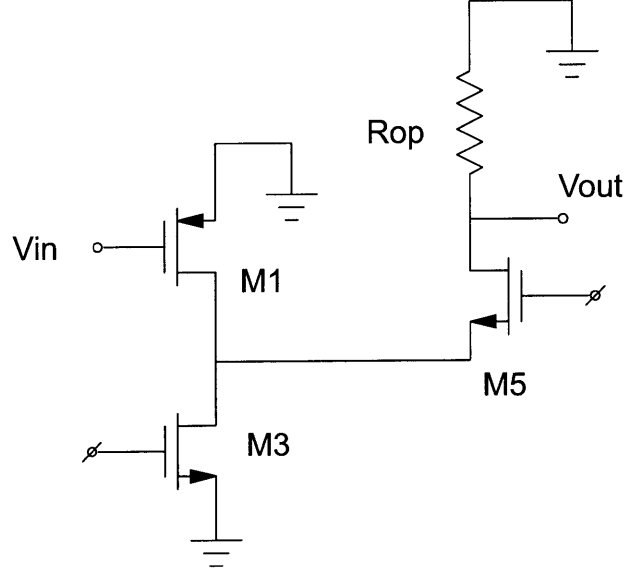


Figure 4-2: Half circuit of folded cascode opamp

V_{b1} and V_{b2} at the gates of $M3$ and $M5$ respectively are assumed to be at analog ground for small-signal analysis.

From figure 4-3, the following current-voltage relationships can be derived:

$$g_{m5}V_{gs5} + \frac{V_o + V_{gs5}}{r_{o7}} = g_{m1}V_i - \frac{V_{gs5}}{r_{o1}/r_{o3}} = -\frac{V_o}{R_{op}}$$

The small signal differential voltage gain is thus given by:

$$Gain = \frac{V_o}{V_i} = -\frac{g_{m1}R_{op}((r_{o1}/r_{o3})(1 + g_{m5}r_{o5}) + r_{o5})}{((r_{o1}/r_{o3})(1 + g_{m5}r_{o5}) + r_{o5}) + R_{op}}$$

To maintain a high overall amplifier output resistance, the current sources I_{b2a} and I_{b2b} are implemented as cascode current mirrors. Their output resistances can be derived using the simplified small signal model as shown in figure 4-4.

$$R_{op} = (1 + g_{m7}r_{o7})r_{o9} + r_{o7}$$

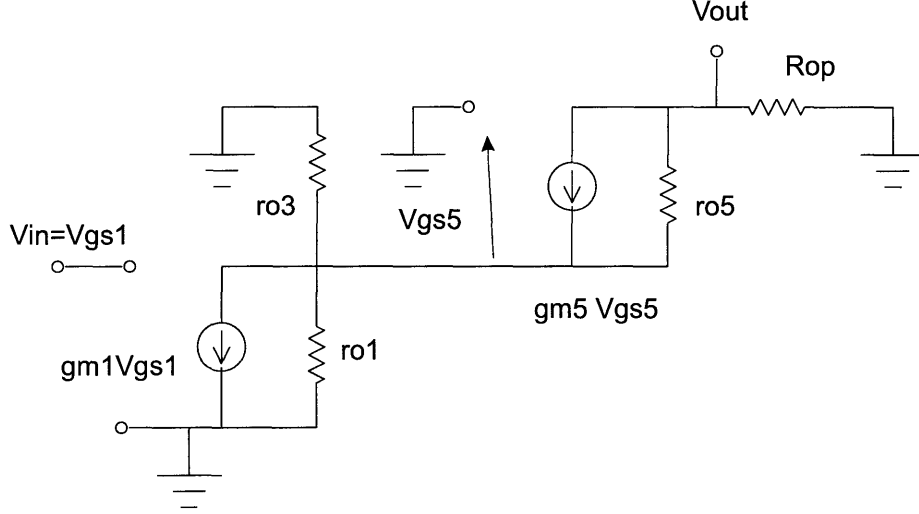


Figure 4-3: Small signal half circuit of folded cascode opamp

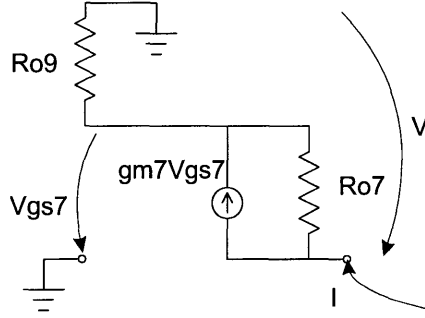


Figure 4-4: Small signal model of cascode current mirror

Another important design criteria is the frequency response. The dominant poles of the amplifier are the ones due to the output load capacitor C_L and the parasitic capacitance C_{L2} seen at the node where the drains of transistors M1 and M3 join with the source of transistor M5.

The first dominant pole for small differential signals is at:

$$f_{p1} = \frac{1}{2\pi(R_{on}/R_{op})C_L}$$

where

$$R_{on} = (1 + g_{m5}r_{o5})(r_{o1}/r_{o3}) + r_{o5}$$

The resistance seen at the node where C_{L2} is located can be found using open circuit time constant analysis:

$$R_{L2} = \frac{(r_{o1}/r_{o3})r_{o5}}{r_{o5} + (r_{o1}/r_{o3})(1 + g_{m5}r_{o5})}$$

Hence the second dominant pole for small differential signals is at:

$$\omega_{p2} = \frac{r_{o5} + (r_{o1}/r_{o3})(1 + g_{m5}r_{o5})}{2\pi C_{L2}(r_{o1}/r_{o3})r_{o5}} \approx \frac{g_{m5}}{2\pi C_{L2}}$$

4.3 Gain Enhancement

To improve the overall gain of the amplifier a feasible way is to boost the output resistance. One possibility would be adding yet another cascode transistor. However the associated further reduction of output swing [56] is undesirable. Another possibility is to use devices with a wider gate lengths which raises the intrinsic output resistances. Unfortunately the high bias currents required for the settling requirement dictates a high penalty in terms of chip area. As a result, the gain enhancement topology, as shown in figure 4-5 is employed.

Without the amplifier A the output resistance seen at the drain of transistor M2 is of the order $g_{m2}r_{o1}r_{o2}$, ignoring that of the biasing current mirror I_{bias} , with the gate of transistor M2 being held at small-signal ground. With the amplifier A in place, the output resistance is raised by a factor equals to the gain of the amplifier to $Ag_{m2}r_{o1}r_{o2}$. The amplifier A provides extra isolation of the drain of transistor M1 from the output node and hence enhances the overall output resistance.

The simplest approach uses a single transistor $MG1$ to implement the amplifier

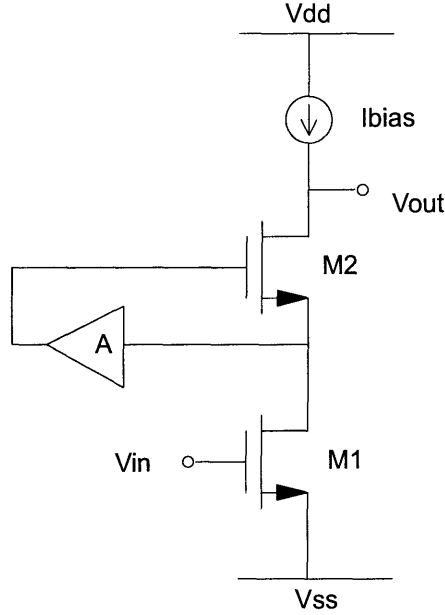


Figure 4-5: Circuit illustrating simple gain enhancement

A shown in figure 4-5. The advantage of the approach, as shown in figure 4-6, is the simplicity of the implementation. However, the gain enhancement is limited to just a fraction of a single $g_m r_o$.

The gain resulting from $MG1$ and current source I_{bg} is $g_{mG1}(r_{oG1}/r_{oIbg})$. In reality I_{bg} is implemented using a single transistor. Its output resistance is thus the transistor's intrinsic output resistance. Here the bias current of $MG1$ is small compared to that of the main amplifier. The transistors making up this gain enhancement topology have long gate lengths to boost their intrinsic output resistances raising the overall output resistance of the active cascode of the order $\frac{1}{2}g_m^2 r_o^3$.

By using a similar approach it is possible to design an amplifier which has an differential small signal gain which has the order $g_m^3 r_o^3$. A simplified circuit schematic is shown in figure 4-7. The devices $MG1$, $MG3$, $MG6$ and $MG8$ are the single transistors that implement the gain enhancement. These transistors, as they are not driving the output capacitance directly, can be biased with smaller bias currents and

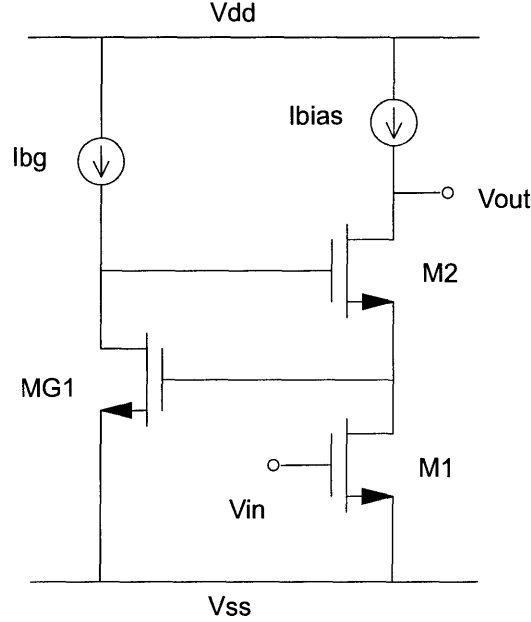


Figure 4-6: Single transistor gain enhancement scheme

their sizes can be chosen such that the extra $g_m r_o$ contributed by them is large.

Another approach is to use a fully differential amplifier to implement the amplifier A, taking advantage of the full differential nature of the design [12, 57]. This topology boosts the output resistance and hence the small-signal differential voltage gain by yet another factor of $g_m r_o$ compared to the previous single-transistor approach. The further increase in complexity, power and chip area was found to be too large. Hence the simple single transistor gain enhancement scheme shown in figure 4-7 was used in all the amplifiers of our design instead.

Figure 4-8 shows the small signal frequency response of the amplifier for a small differential input signal. The low frequency gain is in excess of 80dB and the unity gain bandwidth is about 400MHz and a phase margin of ≈ 50 degrees under a load capacitance of 1pF. This ensures the stability of the amplifier as long as a load capacitance of larger than 1pF is used.

A potential problem of the design is the creation of a high frequency left-half-

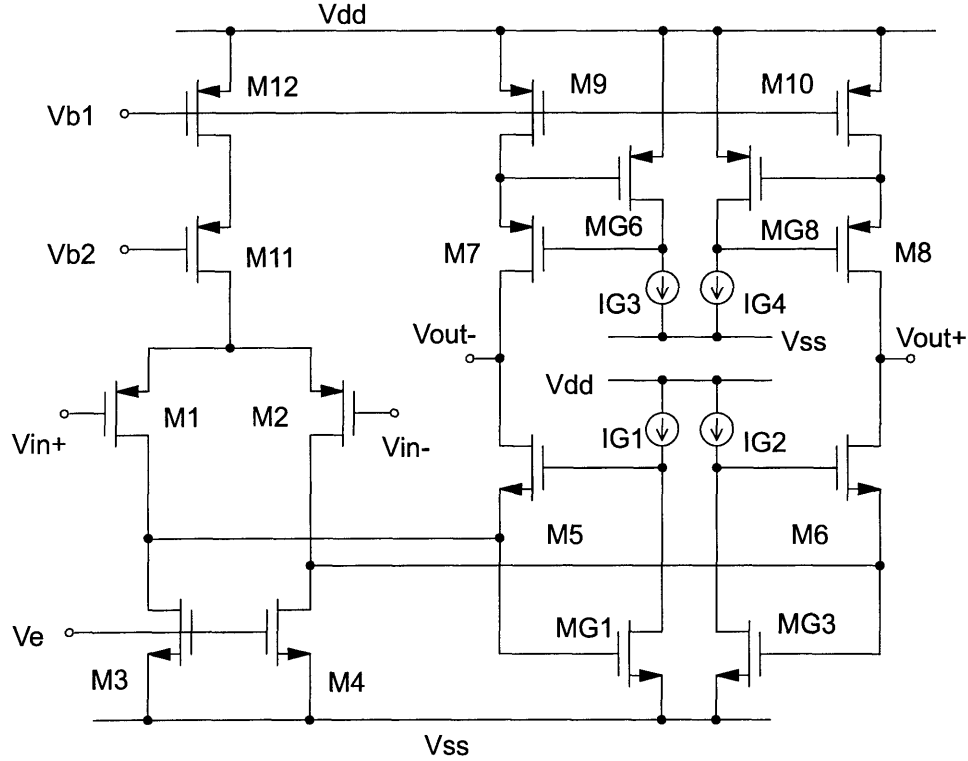


Figure 4-7: Simple gain enhancement amplifier

plane zero. The zero is the result of high frequency signal feeding through transistors $MG1$ and $M5$ to the output. The duplex formed does affect the settling time of the amplifier, possibly lengthening it. However the zero is at such a high frequency that its negative impact on the settling time is not apparent in the amplifier step response as shown in figure 4-9.

4.4 Common Mode Feedback at Outputs

Common mode feedback is necessary to keep the amplifier outputs from saturation. Usually this is implemented at the outputs, i.e. the common mode component of the output voltages is compared with the desired common mode output voltage, in this

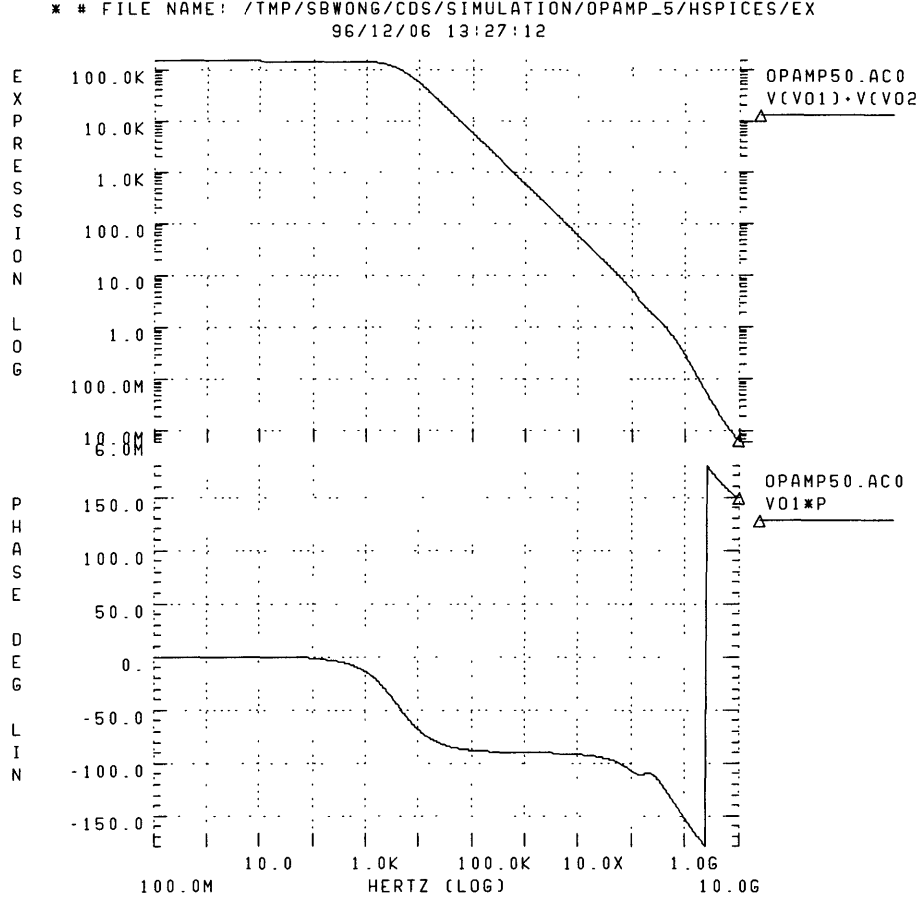


Figure 4-8: Small signal frequency response for a differential input to the amplifier

case the analog ground. This difference is feedback in a way that it is minimized. The circuit level implementation involves a switched-capacitor based scheme as shown in figure 4-10 that derives the common mode component of the output voltages.

Capacitors C_{2a} and C_{2b} form two switched-capacitor "resistors". The periodic sampling keeps the voltage V_c at the mean of V_{out+} and V_{out-} if the capacitor pairs C_1 and C_2 match. In essence the switched-capacitor network forms a RC voltage divider such that $V_c = \frac{1}{2}(V_{out+} + V_{out-})$

Another important component is the differential pair formed by $MC1$ and $MC2$

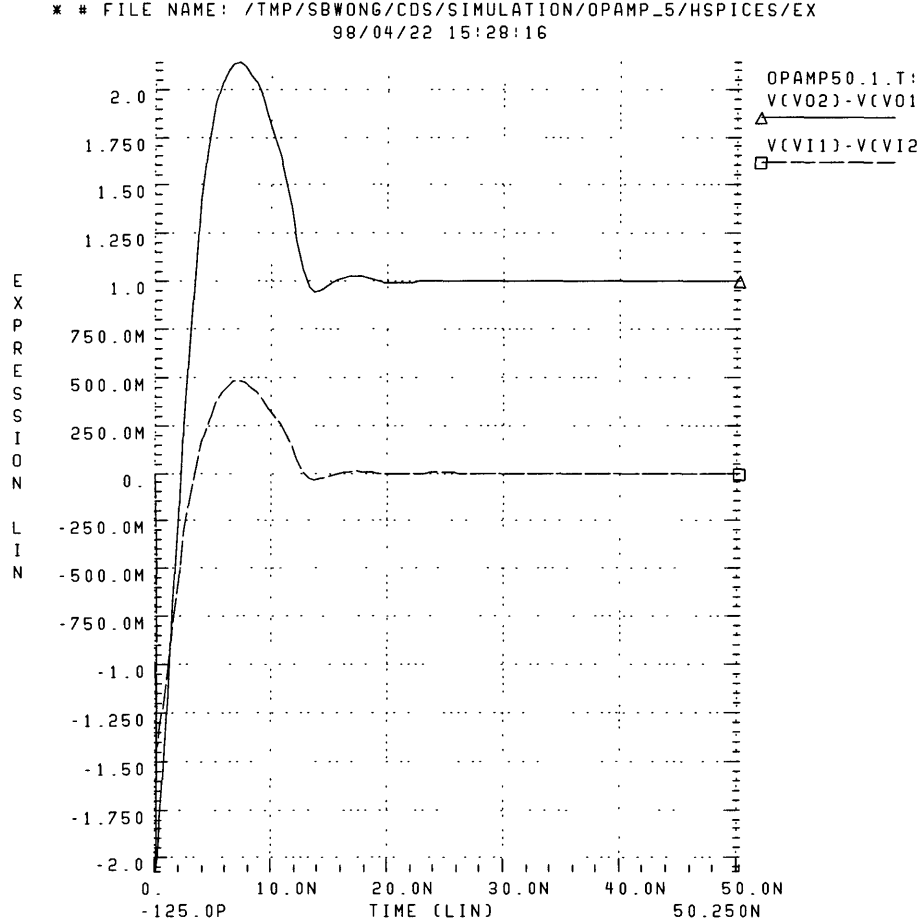


Figure 4-9: Amplifier step response for a 2V differential input, with 1.5pF feedback capacitors, 0.75pF input capacitors and 0.5pF load capacitors

shown in figure 4-11. The common-mode voltage V_c derived from the switched-capacitor network is applied to the gate of $MC2$, while the gate of $MC1$ is tied to the analog ground, the desired common mode output voltage. The difference between these two voltages is converted to a current mirrored via $MC5$ to $M3$ and $M4$. This changes the bias current of the main circuitry supplied by current mirrors $M3$ and $M4$ such that the output common mode voltage V_c tracks the analog ground closely.

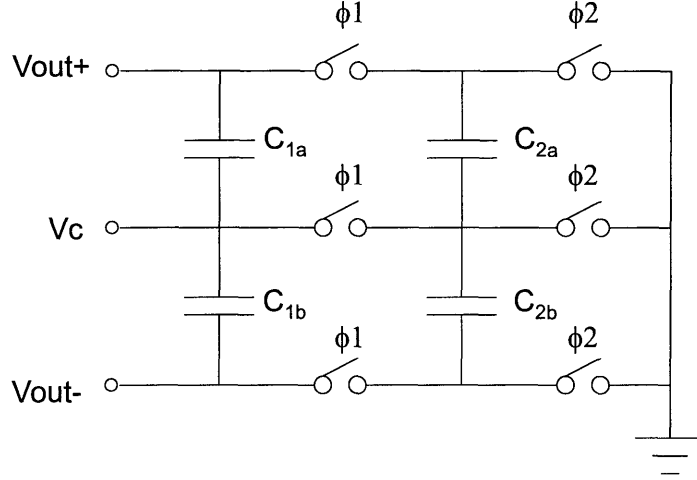
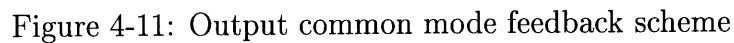


Figure 4-10: Output switched-capacitor based common mode feedback scheme

The stability of the common mode loop is also analyzed similar to that of the differential loop. The design was done such that the common mode loop has a lower gain and a lower unity gain frequency compared to the differential mode loop. With a load capacitance of 10pF, the common mode loop has a low frequency gain of approximately 100dB, a unity gain frequency of 25MHz and a phase margin of 70 degrees compared to 110dB gain, 150MHz unity gain frequency and a 55 degrees phase margin of the differential loop.

4.5 Common Mode Feedback at Inputs

Common mode feedback at the inputs of the amplifier is necessary for the proper functioning of the guard and sense electrodes switching for the displacement sensor. The aim is to maintain the common mode voltage at the inputs to be as close to the analog ground voltage as possible. Then as the sensing electrodes are switched between the reference voltage and the amplifier inputs, the charges carried by the sense capacitances are transferred completely to the integrating capacitors.



Refer to figure 4-12 for the simplified schematic of the device-level implementation. Device M_{13} , with its gate terminal tied to the desired common mode input voltage, shares the same sources terminal as devices M_1 and M_2 that forms the input differential pair for differential input voltages. Consequently for common mode input voltages M_{13} forms a differential pair with both M_1 and M_2 . The size and the bias current for M_{13} are chosen to be the same as that of M_1 and M_2 . Here the addition M_{13} does not alter the inherent symmetry of the differential amplifier.

Consequently a similar half circuit approach can be applied here as earlier in this chapter. For differential input voltages, the amplifier gives the same differential

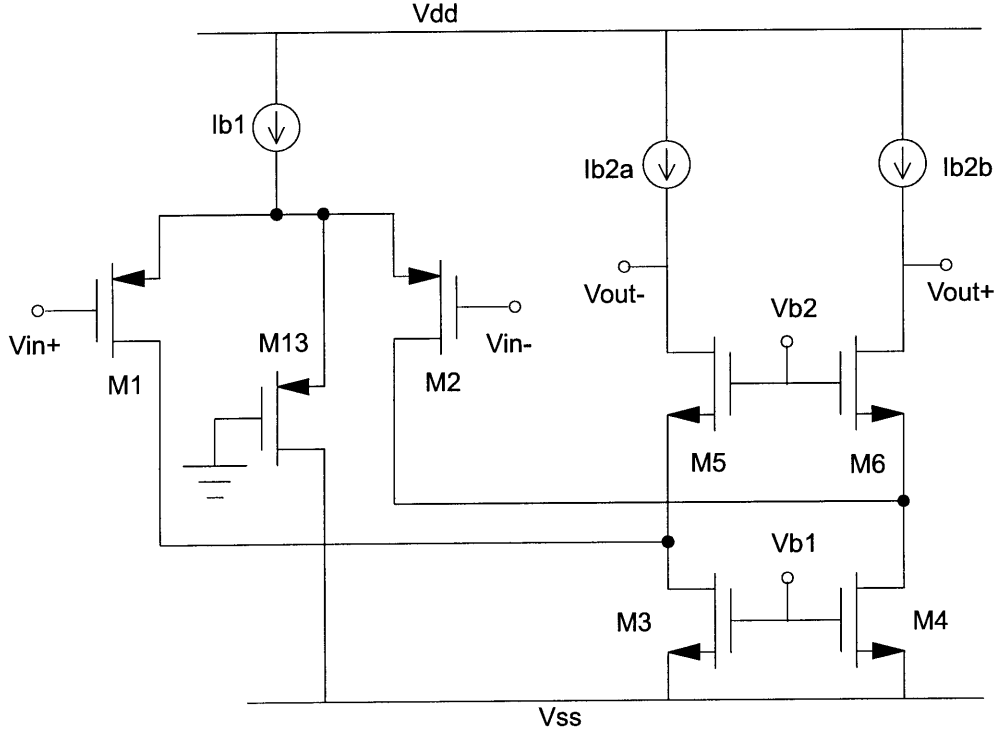


Figure 4-12: Input common mode feedback scheme

voltage gain given as:

$$Gain = \frac{V_o}{V_i} = -\frac{g_{m1}R_{op}((r_{o1}/r_{o3})(1 + g_{m5}r_{o5}) + r_{o5})}{(r_{o1}/r_{o3})(1 + g_{m5}r_{o5}) + r_{o5} + R_{op}}$$

Concerning the differential mode frequency response, the first dominant pole located at the same position as before:

$$\omega_{p1} = \frac{1}{2\pi(R_{on}/R_{op})C_L}$$

However the second dominant pole is shifted because now the output node V_o deviates from small signal ground unlike in the previous case where common mode feedback forces V_o to be at small signal ground. Using a similar open circuit time

constant analysis the second dominant pole frequency is found to be:

$$\omega_{p2} = \frac{1}{2\pi C_{L2} \left(\frac{r_{o5} + R_{op}}{1 + g_{m5} r_{o5}} // r_{o1} // r_{o3} \right)} \approx \frac{3}{2\pi C_{L2} r_o}$$

Consider the circuit for input common mode voltages. Due to the inherent symmetry the half circuit concept can be applied which gives a simplified small signal model as shown in figure 4-13.

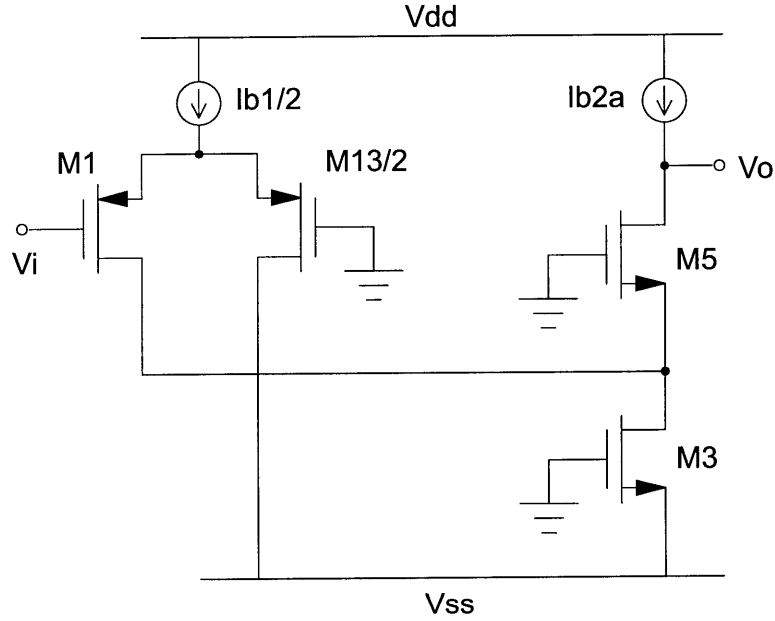


Figure 4-13: Simplified Small Signal Circuit for Common Mode Feedback at Inputs

For small-signal analysis, transistor $M13/2$ can be considered as a resistance $\frac{1}{g_{m13/2}}$ to the small signal ground. Hence its effect is to reduce the common mode loop gain in a manner similar to that of a source degeneration resistor. The low frequency small-signal gain was found to be $\frac{g_m^2 r_o^2}{7}$. The frequency response is essentially dominated by the low frequency pole due to the load capacitance C_L connected at the output. The second pole was found to be at a higher frequency compared to that of the differential loop. Hence the stability of the differential loop essentially guarantees

that of the common mode loop.

4.6 Choppers at Inputs and Outputs

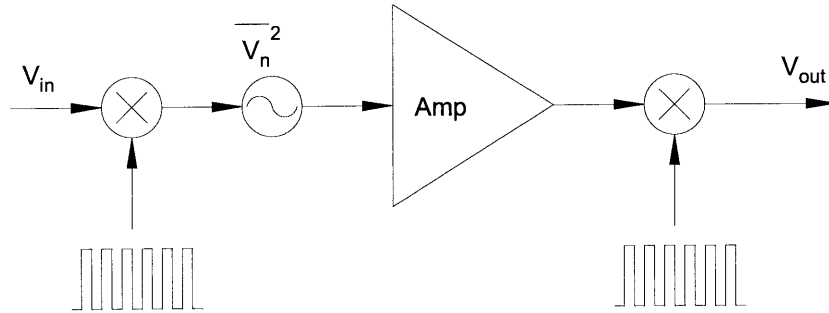


Figure 4-14: Illustration for the chopper stabilized amplifier concept

To counter the dc offset and low frequency noise problems, choppers [58, 59] are used. The basic idea behind chopping is illustrated in figure 4-14. Before a signal is passed through an amplifier it is multiplied by a square wave at a frequency f_{chop} . This shifts the signal spectrum such that it is centered about f_{chop} . The modulated signal is then passed to the amplifier which combines this modulated signal with its own noise spectrum, comprising of wideband thermal noise and low frequency flicker noise. The output signal from the amplifier is then multiplied by the same square wave as used before amplification thus returning the signal spectrum to its original low frequency location. Now the low frequency flicker noise from the amplifier is modulated to frequencies about f_{chop} . Consequently the amplifier flicker noise is effectively removed from the baseband signal.

As all low frequency noise peaks will be relocated to odd multiples of the chopping frequency f_{chop} the chopping frequency is selected to be half of the sampling rate. This ensures that no aliasing of the shifted noise peaks back into the pass band during any subsequent sampling at the clock rate.

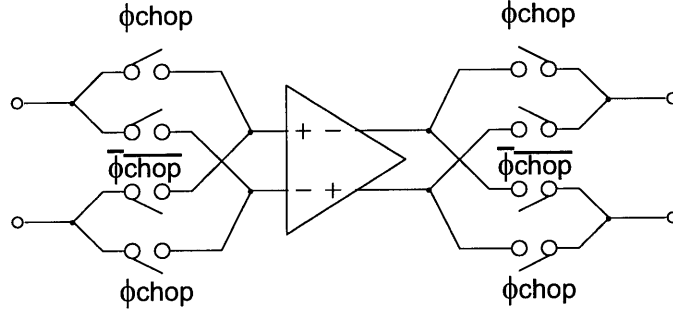


Figure 4-15: Implementation of choppers

The implementation of the choppers is shown in figure 4-15. Essentially the multiplication is performed by 4 complementary switches comprising of transistors having minimize sizes to lower the effect of charge injection. The differential nature of the design makes the use of 4 complementary switches feasible as the differential signal entering and leaving the amplifier can be inverted by simply exchanging the two inputs.

4.7 Opamp Noise Considerations

The use of a fully differential design and choppers reduce low frequency noise, for example $\frac{1}{f}$ noise. However the effect of wide band thermal noise can often be much more important than that of the $\frac{1}{f}$ noise. These are considered in this section.

To achieve the desired resolution specifications of the modulator, the input referred noise of the amplifiers have to be minimized. To do so, the transconductance g_m of the devices making up the input differential pair has to be large. This is because the noise contributions of the other devices making up the amplifier are divided by this g_m when referred to the input. Consequently a large bias current and large geometry devices are used as the PMOS differential pair.

The procedure is to assume the noise generated by each device (thermal noise

of the drain current and flicker noise of the drain current) can be represented by an equivalent noise source $\overline{V_{nieq}^2}$ connected to its gate. Then the output voltage due to that particular noise source can be calculated. By summing up contributions from each device making up the amplifier, assuming the different noise sources are not correlated with each other, we can derive the total output noise voltage $\overline{V_{nout}^2}$. Finally, dividing the $\overline{V_{nout}^2}$ by the differential voltage gain of the amplifier will give us the total input referred noise.

Under the assumption that flicker noise is removed by chopping, the only noise source for each device is the thermal noise associated with the drain current. Thus,

$$\overline{V_{nieq}^2} = \frac{8kT}{3g_m} \Delta f$$

The analysis yields the following equivalent input referred noise:

$$\overline{V_{nieq(amp)}^2} \approx \overline{V_{n1,2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \overline{V_{n3,4}^2} + \left(\frac{1}{g_{m1}r_{o3}}\right)^2 \overline{V_{n5,6}^2} + \left(\frac{1}{g_{m1}r_{o3}}\right)^2 \overline{V_{n7,8}^2} + \left(\frac{g_{m9}}{g_{m1}}\right)^2 \overline{V_{n9,10}^2}$$

All the terms that contribute to the overall input referred noise of the amplifier involve g_{m1} in the denominator. Hence, to have a low noise amplifier it is required to have g_{m1} to be as large as possible. In addition, the transconductances of the transistors $M3$, $M4$, $M9$ and $M10$ have to be minimized in order to lower the overall input referred noise. The tradeoff here is that the input differential pair is made up of PMOS transistors which have a lower transconductance compared to their NMOS counterparts. The choice was made due to open loop stability considerations as described in section 4.2. Also the terms that involve the contributions from transistors $M5$, $M6$, $M7$ and $M8$ are small compared to the other terms and their effects can be ignored, giving rise to:

$$\overline{V_{nieq(amp)}^2} \approx \overline{V_{n1,2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \overline{V_{n3,4}^2} + \left(\frac{g_{m9}}{g_{m1}}\right)^2 \overline{V_{n9,10}^2}$$

A summary of the performance of the opamp is given below:

Low frequency ac gain	86dB
Unity gain bandwidth (1pF load)	400MHz
Open loop phase margin (1pF load)	50 degrees
Maximum output current	700 μ A
Total input referred thermal noise	1.73nV/ \sqrt{Hz}
Total bias current	5.46 mA
Settling time (0.1%)	25ns
Area	350 $\mu m \times$ 560 μm

Chapter 5

Circuit Implementation

The prototype we have implemented is a fully differential switched-capacitor based design. The layout design was performed such that the individual blocks, namely the capacitance-to-voltage conversion circuitry and the 5th order modulator can be independently tested. To do so, 2 pins of the DIP28 package were doubled as the output of the C-V conversion circuitry and also the inputs to the modulator. One drawback of this approach is the increased capacitive load due to the package at the C-V conversion circuitry outputs, possibly leading to an increased settling time and hence lower the potential master clock speed for the on-chip switched-capacitor circuitry.

5.1 Capacitance-to-Voltage Conversion

The C-V conversion circuitry interfaces to the sense electrodes of the capacitance displacement probes. The aim is to have the varying capacitance due to displacement changes converted to a differential voltage output such that the magnitude of the voltage output is a representation of the varying capacitance. A fully differential

topology is used to reduce common mode non-idealities.

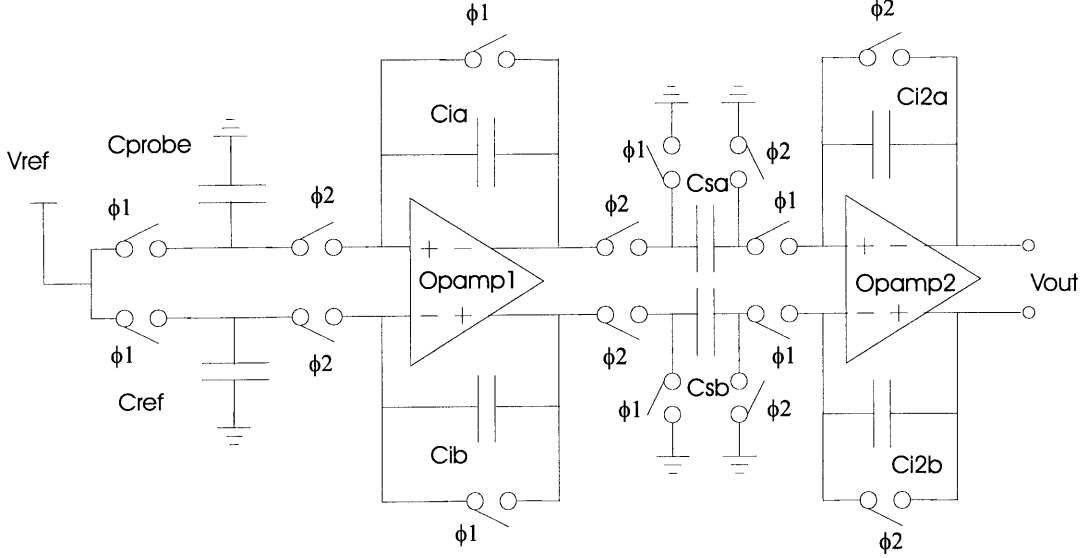


Figure 5-1: Capacitance-to-voltage conversion circuitry

Referring to the circuit schematic shown in figure 5-1. Opamp 1 is the amplifier that has common mode feedback at the inputs as described in section 4.5 whereas opamp 2 is an amplifier that has output common mode feedback. Common mode feedback at the inputs of opamp 1 ensures that the voltage levels of the inputs always stay close to the common mode reference voltage, in this case the analog ground voltage. Hence the sense capacitor C_{probe} , and the dummy reference C_{ref} , are switched between the reference voltage V_{ref} and the analog ground voltage. As a result, the design of the guard drives is simplified to switches connecting the guard pins to V_{ref} and analog ground voltage. As a result, after the transients die away, the guard and the probe are both driven to the same voltage and hence the parasitic capacitance between them is boot-strapped out.

During ϕ_1 , C_{probe} and C_{ref} are connected to V_{ref} while the integrating capacitors C_i 's are discharged. During ϕ_2 the charges on C_{probe} and C_{ref} are transferred to the respective C_i 's, giving rise to a differential output voltage directly proportional to the

difference in capacitance between C_{probe} and C_{ref} . However the common mode output voltage is large due to the large common mode component of the capacitance being measured. Here opamp 2 with C_s and C_{i2} forms a gain block to scale the differential voltage to fit the operating range of the modulator input while rejecting the common mode voltage at the outputs of opamp 1.

In the design, capacitors C_{1a} and C_{1b} were chosen to be 15pF. Given a maximum amplifier output swing of $\pm 1.5V$ the maximum input capacitance, plus the associated parasitic capacitance in parallel with it, is 9pF. The desired range of capacitances to be measured has a maximum of 3.48pF and hence the internal nodes of the C-V conversion circuitry are not going to saturate.

5.2 5th Order Modulator

The 5th order modulator forms the core for the analog-to-digital implementation of our prototype chip. The implementation is switched-capacitor based and fully differential. The modulator outputs a bit stream that is synchronized to the ϕ_2 clock signal. Each modulator coefficient, namely b 's, c 's and γ 's, shown in figure 3-10 is implemented by ratio of capacitors. A simplified circuit schematic for the modulator is shown in figure 5-2, which contains 5 fully-differential opamps and hence 5 integrators and a 5th order implementation. Individual components and their implementation will be given below.

5.2.1 Integrator

The modulator has 5 integrators and hence 5th order. Each integrator implements the transfer function $\frac{z^{-1}}{1-z^{-1}}$ in figure 3-10. Individual gain c of an integrator can be set by the capacitor ratio $\frac{C_s}{C_i}$ as shown in figure 5-3.

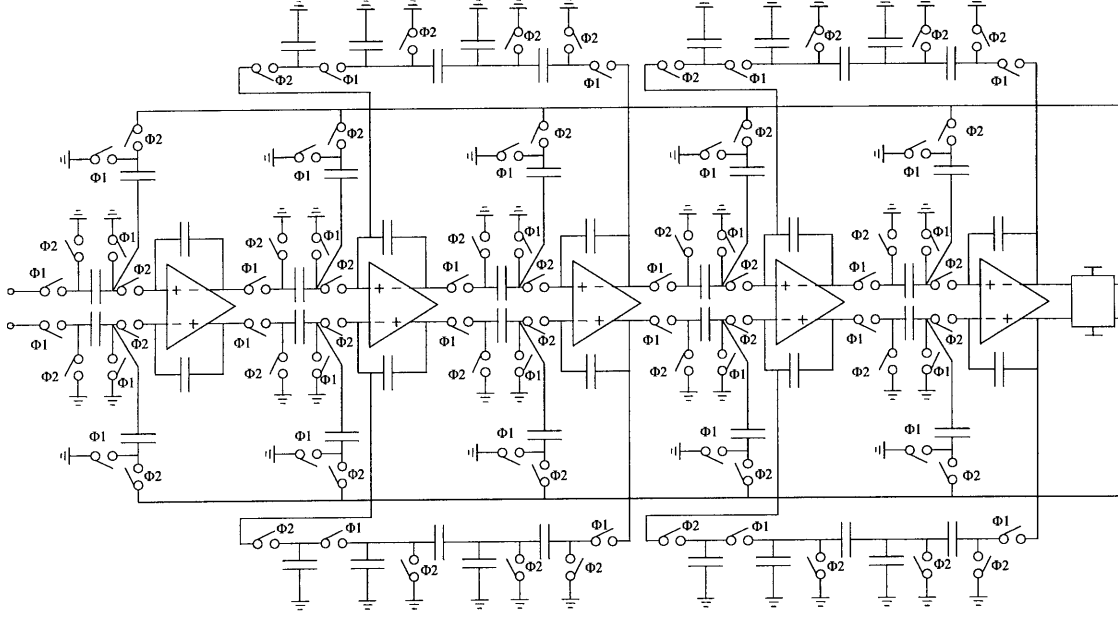


Figure 5-2: 5th order modulator simplified schematic

Consider only the top half of the circuit in figure 5-3. During ϕ_1 , C_s is charged to V_{in+} . Assuming charge conservation, the charge on C_s is transferred to C_i during ϕ_2 such that the output voltage V_{out+} increases by $\frac{C_s V_{in+}}{C_i}$. In the Z-domain,

$$\frac{V_{out+}}{V_{in+}} = \frac{C_s}{C_i} \frac{z^{-1}}{1 - z^{-1}}$$

5.2.2 Small Coefficients for Zeros

The design uses noise shaping zeros at low frequencies with tiny resulting γ coefficients. A limit exists on the smallest capacitor size that can be realized due to parasitic considerations. If the γ 's are to be realized by ratio of a single pair of capacitors the larger capacitor will have too large a size. The approach adopted by S. Nadeem [60] shown in figure 5-4 was adopted instead.

Figure 5-4 shows a single-ended implementation where the opamp and the capac-

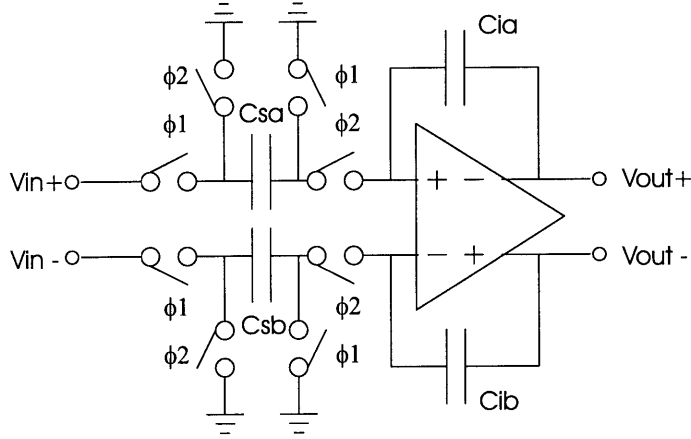


Figure 5-3: Differential switched-capacitor integrator

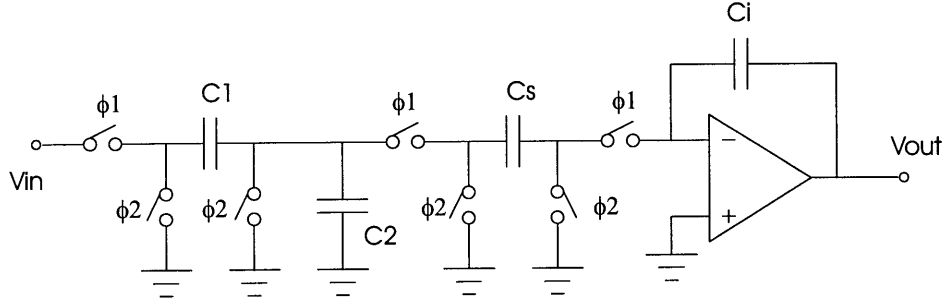


Figure 5-4: Implementation of small coefficients

itor C_i forms an integrator. During ϕ_2 the capacitors C_1 , C_2 and C_s are connected to analog ground and fully discharged. During ϕ_1 , C_1 , C_2 and C_s are connected to form a capacitive divider. Using charge conservation the equivalent ' C_s ' can be derived:

$$C'_s = \frac{C_s C_1}{C_1 + C_2 + C_s} \approx \frac{C_s C_1}{C_1 + C_2}$$

Assuming $C_1, C_2 \gg C_s$.

In the actual implementation, this approach was extended to implement the tiny γ 's, as shown in figure 5-5. The extension was necessary to generate reasonably sized C_1 's and C_2 's for the γ 's chosen. In essence we have two capacitive dividers cascaded

together to implement the small coefficient.

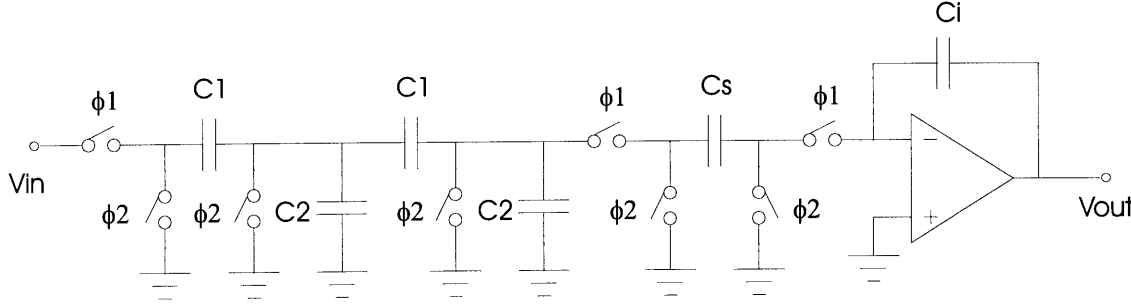


Figure 5-5: Actual circuit implementation of small coefficients

Assuming $C_2 \gg C_s$ the loading effect of C_s can be neglected. Using charge conservation the new equivalent ‘ C_s' ’ can be determined:

$$'C_s' \approx \frac{C_s C_1^2}{(C_1 + C_2)^2}$$

This scheme is not parasitic insensitive. Thus, the stray capacitances set a limit on the minimum size capacitor that can be used. Simulations determined that the γ 's can be varied by a factor of 10 before the conditional stability of the modulator is compromised.

5.2.3 Single-Bit Comparator

A fully differential single-bit comparator that has a high decision speed and low decision ambiguity is desirable. A dynamic pull up pull down latch used successfully in similar modulator implementations [5, 12] and also in static memory designs [61] was chosen due to its relatively simplicity and small chip area consumption. The effect of the offset of the latch is not important because when it is referred to the modulator input, its effect is divided by the high gains of 5 integrators in cascade.

Figure 5-6 shows the schematic for the latch, which consists of two clocked back-

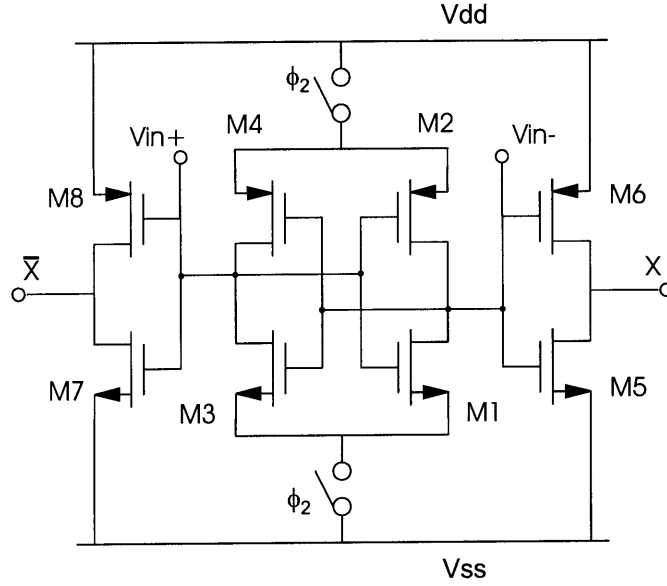


Figure 5-6: Comparator circuit schematic

to-back inverters consists of transistors M_1 to M_4 . When the clock ϕ_2 is inactive these two inverters are floating such that differential input voltages are set on the nodes V_{in+} and V_{in-} . When ϕ_2 is active initially a small differential voltage exists between V_{in+} and V_{in-} . This difference is quickly amplified by the positive feedback action of the back-to-back inverters. Thus after some small delay a steady state is reached where one of the two nodes will be pulled high whereas the other node will be pulled low. Transistors M_5 to M_8 form two extra inverters to buffer the differential outputs X and \bar{X} .

5.2.4 Distributed Differential Feedback

The feedback portion of the modulator is another important component. Here a differential structure is required due to the differential nature of the modulator. One possible implementation uses two voltage references, namely one positive and one negative voltage reference, such that the capacitors implementing the feedback co-

efficients are switched between one of these references depending on the comparator output. A major drawback is that the two voltage references must match well, i.e. if the positive reference outputs a voltage V_{ref} the negative reference has to output $-V_{ref}$. Otherwise a differential signal will be injected into the modulator from the distributed feedback. And this differential signal is not distinguishable from the differential input signal that we are interested in.

The problem with matched positive and negative voltage references can be overcome by using a single positive voltage reference [5]. As the modulator is switched-capacitor based, by a careful arrangement of the switching sequence of the switches as shown in figure 5-7, a positive or a negative coefficient can be implemented. In particular consider the top feedback capacitor C_{fb1} . During ϕ_1 it is charged to V_{ref} . During ϕ_2 , it is discharged such that charges are taken out from the virtual ground node. On the other hand, the bottom feedback capacitor C_{fb2} is fully discharged during ϕ_1 . It is then charged during ϕ_2 depositing charges into the virtual ground node. The only difference between top and bottom feedback capacitors is the switching sequence of their associated switches.

Another advantage of the scheme is that no matter what the comparator decision is, the load on the single positive voltage reference V_{ref} is the same. Hence loading effects associated with comparator decision are largely eliminated.

In figure 5-7, the comparator outputs X and \overline{X} are buffered using 2 *AND* gates. Another input of the *AND* gate is the clock signal ϕ_2 . As the comparator will exhibit some delay before reaching a final decision, this ensures that feedback capacitors are not connected to any of the virtual ground nodes of the integrators before a valid comparator decision is reached.

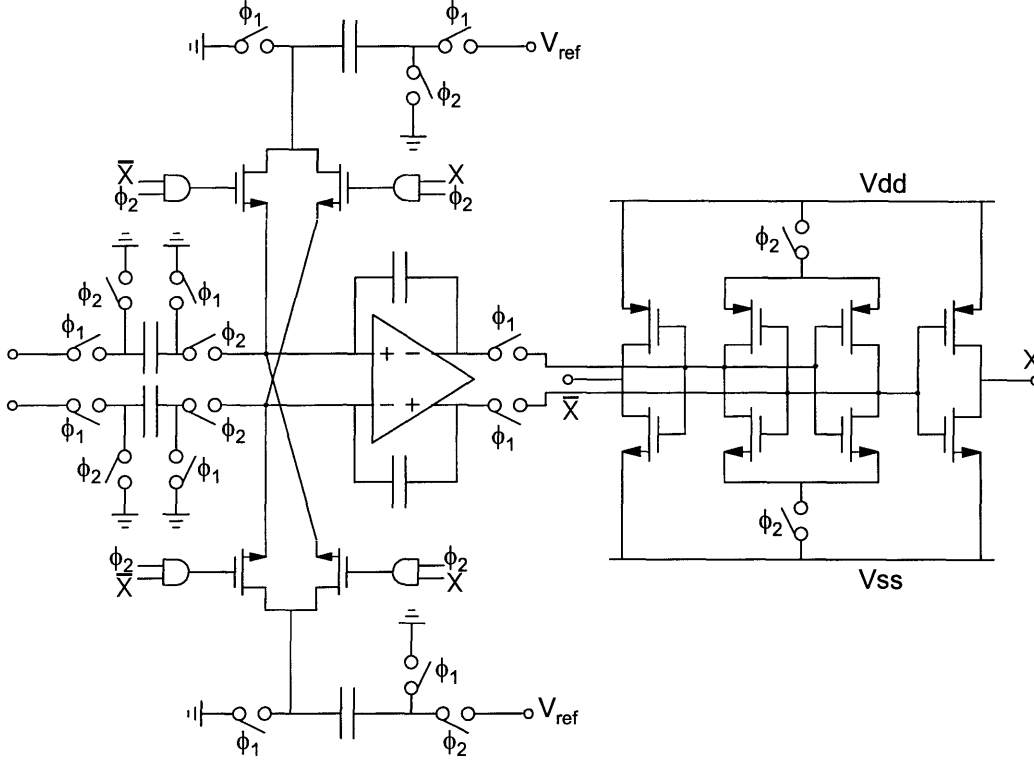


Figure 5-7: Differential feedback scheme and single-bit comparator

5.3 Layout

One of the most important task of an IC design is the layout design. This process transforms circuit schematic to geometrical shapes on different layout layers. Figure 1-2 shows the layout of our prototype chip.

5.3.1 Pin Assignment

The DIP28 package was chosen to provide sufficient number of I/O pins for our design. The main consideration is that the interface of the C-V frontend to off-chip components is as symmetrical as possible. This ensure that the parasitic capacitances associated with the differential capacitance inputs of the C-V frontend are matched.

In addition, the design uses six off-chip clock signals. They enter the package at the opposite side to the C-V frontend inputs such that their interference to the sensitive analog circuitry is minimized. As shown in figure 1-2, the clock signals enter the die from the top whereas the off-chip capacitors enters from the bottom.

5.3.2 Opamps

Matching is also important for the opamps. Each transistor pairs making up the design was constructed from numerous smaller unit devices connected in parallel, and arranged in a common centroid geometry such that a first order cancellation of process variations is achieved [59].

5.3.3 Capacitors

Metal 1-Polysilicon capacitors are used throughout in the design. Their absolute value is not well known as the oxide thickness between Metal 1 and Polysilicon is not a well controlled process parameter. This does not, however, represent a major problem because our design, except the C-V frontend, depends on capacitor ratios rather than absolute capacitor values. Consequently the integrating capacitors of the C-V frontend assume values that are larger than necessary.

The capacitor pairs were implemented using a common centroid design to improve the matching within the pair. The unit capacitor approached [59] was not used as the tolerance required to achieve a desired capacitor ratio in the modulator design such that the extra routing and area consumption was not considered to be justified.

All sensitive nodes of the design are connected to the metal 1 layer of the capacitors. The polysilicon layer has large associated parasitic capacitances to the substrate such that they are connected to the less sensitive nodes instead.

One possible problem associated with the on-chip capacitors is the voltage de-

pendency of their absolute values. This can translate into deviations of the capacitor ratios from their design values, thus causing changes in the modulator signal and noise transfer functions. Consequently the noise-shaping performance of the modulator can be compromised.

5.3.4 Electrostatic Discharge (ESD) Protection

ESD protection was used for all the package pins except the C-V frontend input pins. This is a compromise between static discharge protection and the desire to have as few components connected to the differential capacitance inputs as possible. The circuit schematic (from T.Adams [62]) is shown in figure 5-8

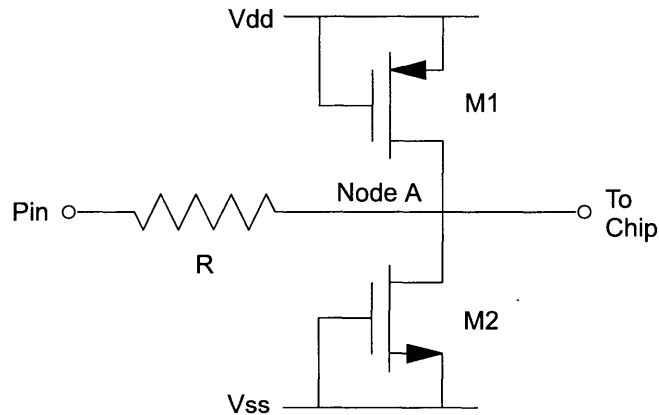


Figure 5-8: ESD protection circuitry

If the voltage on a package pin is forced more than a threshold voltage above V_{dd} , transistor $M1$ will turn on and drive node A to V_{dd} . Similarly, if the pin voltage is more than a threshold voltage below V_{ss} , $M2$ will turn on and drive node A to ground. The resistor R provides high current protection through a voltage drop.

Chapter 6

Results

This chapter presents simulated and measured results from our first prototype. We show that both the capacitive-to-voltage conversion and the sigma-delta modulator portion of the chip are operational. However the noise level is much higher than anticipated. We also try to explain the observed noise level.

6.1 Simulation Results

Extraction on the chip layout gives rise to a HSPICE representation of the chip that can be simulated. The two main functional components were simulated independently. Simulated transient behavior was checked off against expected theoretical behavior.

6.1.1 Capacitance-to-Voltage Conversion Circuitry

Simulations were used to verify settling and functionality of this building block. As mentioned previously the internal nodes at the output of *opamp1* in figure 5-1 bear the largest capacitive load due to the limited voltage swings of the opamp implementation. Settling of these two nodes is one important design criterion. Transient simulations

were run using the different publicly available MOSIS models. However the layout extraction program has built-in limitations that only some parasitic capacitances are extracted. Consequently the simulated results were only a rough approximation of the actual circuit behavior.

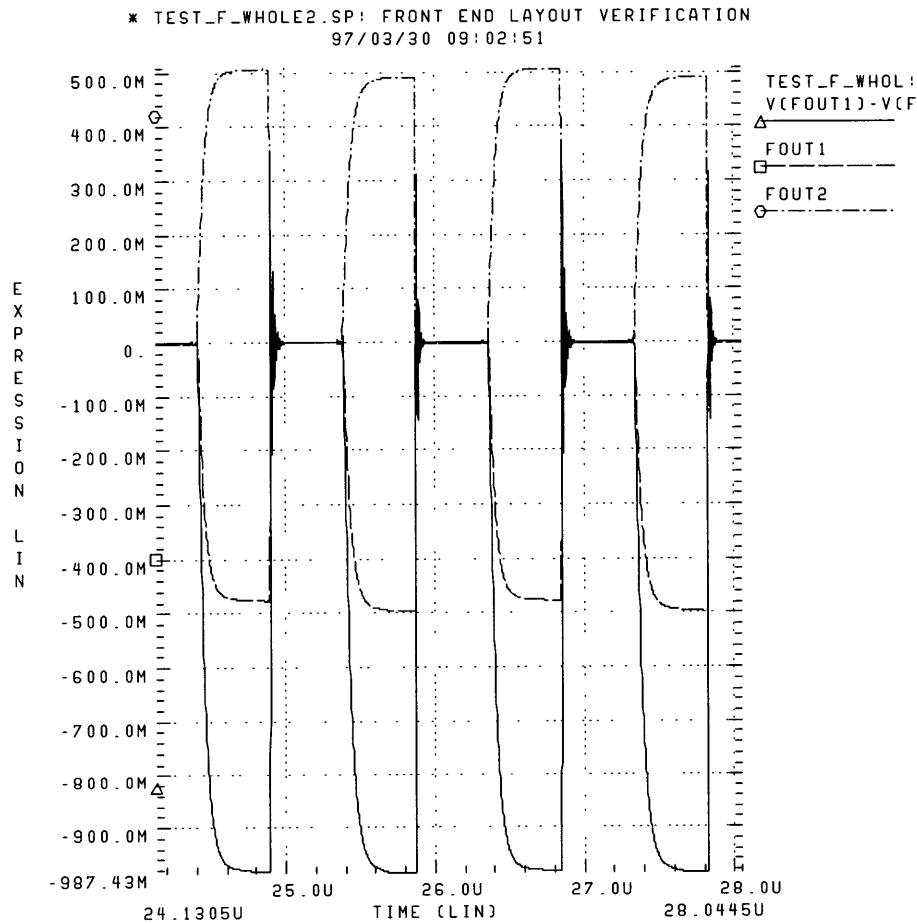


Figure 6-1: HSPICE simulated capacitance-to-voltage circuitry outputs

Figure 6-1 shows the transient response of the outputs of the capacitance-to-voltage conversion circuitry, with input capacitors being 3.5pF and 2.3pF, and an extra 3pF to ground in parallel to each input capacitor. The final value of the differential output voltage is approximately 1.0V confirming the theoretical capacitance-

to-voltage gain of 0.8333V/pF .

In addition, functional verification was also performed by varying the value of the ‘probe’ capacitance and observing the corresponding change in the output differential voltage. Simulation results, however, do not necessarily correspond to the measured results. A possible reason is that the layout extractor limitation as mentioned before. Another one is that the metall-polysilicon oxide thickness, and hence the absolute capacitance-per-unit-area value of the metall-polysilicon capacitors used, is not a very well controlled process parameter. This does not represent a problem for normal switched-capacitor implementations as capacitance ratios are not affected although absolute values of each capacitor deviate from the design values. However, here the off-chip ‘probe’ capacitances do not scale with the integrating capacitors of *opamp1*. As a result, the differential output voltages vary from chip-to-chip due to process variations. Calibration can solve this problem, provided no clipping occurs within the internal circuit nodes.

6.1.2 5th Order Modulator

Transient simulations were run to generate sufficient data points to calculate the modulator spectrum. A tradeoff exists between the number of data points obtainable and the simulation time. A differential sinusoidal input signal of an amplitude smaller than the conditional stability limit was used. Several simulations were run with different input frequencies and amplitudes.

Here, simulation using HSPICE was only suitable for a quick check on the layout implementation. Simulation accuracy, similar to that outlined in section 3.4.4, dictates that the implemented modulator spectrum, and thus the signal-to-noise ratio cannot be easily determined. In addition, the limited computing resources available placed a hard limit on the length and the number of simulations that can be per-

formed. Consequently the modulator stability, on the layout level, cannot be fully verified.

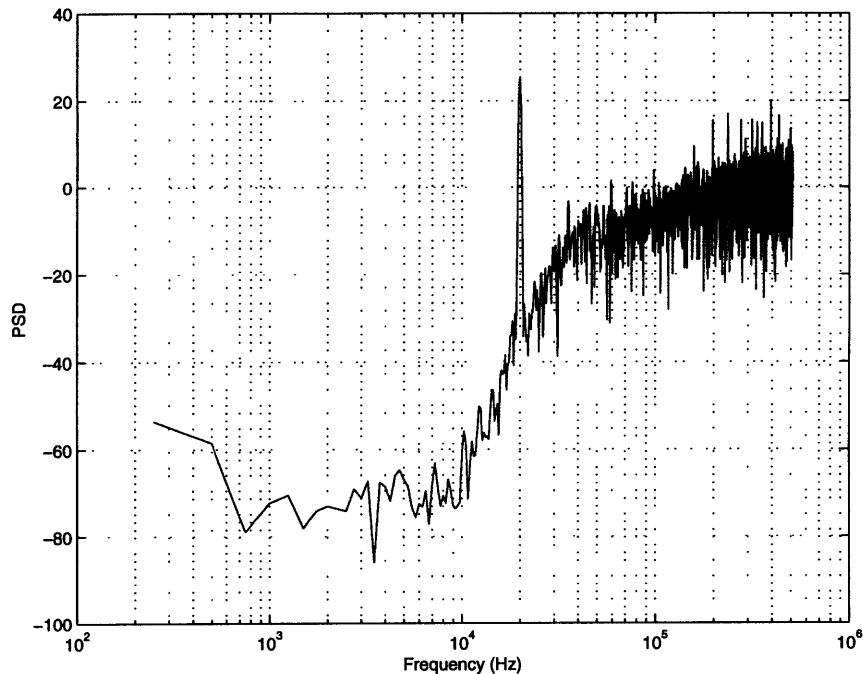


Figure 6-2: Simulated modulator spectrum using HSPICE transient simulation, with input being sinusoidal signal at 20kHz 2.8V peak-to-peak, 4096 data points

The HSPICE transient simulation was set up such that the modulator output voltage mod_{5out} was sampled at approximately a quarter of a clock cycle after ϕ_2 becomes active. This ensures mod_{5out} is completely settled when sampled. A Hamming window having the same length as the data was convolved with the data to obtain the windowed version of mod_{5out} . Finally a Fast Fourier Transform was taken on the windowed data and the power spectral density plots as shown in figures 6-2 and 6-3 were generated using 8192 data points. From these figures, the input signal can be clearly seen as a single spike. In addition, the high frequency noise shaping characteristics were confirmed, namely, the slope of the spectrum matches closely with that from SWITCAP2 simulations.

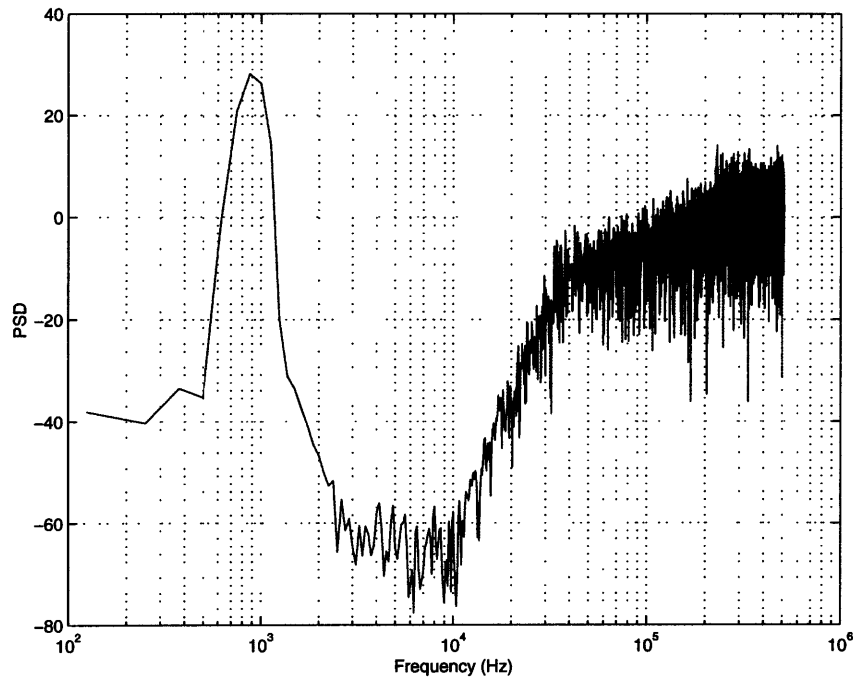


Figure 6-3: Simulated modulator spectrum using HSPICE transient simulation, with input being sinusoidal signal at 800Hz 2.8V peak-to-peak, 8192 data points

From figure 6-2 the noise shaping characteristics of the modulator and the input signal itself is evident. This can be seen also in figure 6-3. However the low frequency portion of both spectra are not clear. The limited number of data points available from the simulation limits the frequency resolution obtainable. In addition, using a low frequency sinusoidal input is not very feasible because it will take too many data points, and consequently very long simulation time, before even one single cycle of the input signal is completed. There is a tradeoff between simulation time and the amount of simulation data obtainable.

HSPICE transient simulations also suggest a noise floor significantly higher than that predicted theoretically. One possible explanation is due to simulation accuracy. It was found that by tightening the accuracy of the simulation, the resulting waveform for mod_{5out} is different from those obtained with the accuracy more relaxed. However,

tightening the simulation accuracy leads to an enormous increase in the simulation time which is not feasible given the limited computation resources available.

6.2 Measured Results

Numerous measurements were taken on our prototype chip fabricated by MOSIS. The data collected was compared with the simulated and theoretical results.

6.2.1 Test Board Implementation

Voltage references, current biases and clock generation circuitry were not included in our prototype chip to enable flexibility in testing. This means that they have to be generated externally. To carry these components, a five-layer analog test board was designed using the ACCEL EDA package.

Voltage References

For our prototype chip, two precision positive references are required: one for the C-V front-end circuitry, and one for the modulator. An Analog Devices *AD780* precision voltage reference is used directly since it can supply the currents required for charging up the on-chip capacitive loads. No extra buffering is used due to noise considerations.

In addition, the prototype chip requires 2 separate analog and digital split $\pm 2.5V$ supplies. The separate supplies ensures that voltage spikes due to on-chip digital circuitry do not get coupled onto the analog supplies. These supply voltages are generated on the analog test board as shown in figures 6-4 and 6-5.

Relatively large current loads are required on these supplies. The precision voltage generated by an *AD780* precision voltage reference is buffered using an *OP07* opamp and a bipolar transistor. Stability analysis was performed to ensure stable operation.

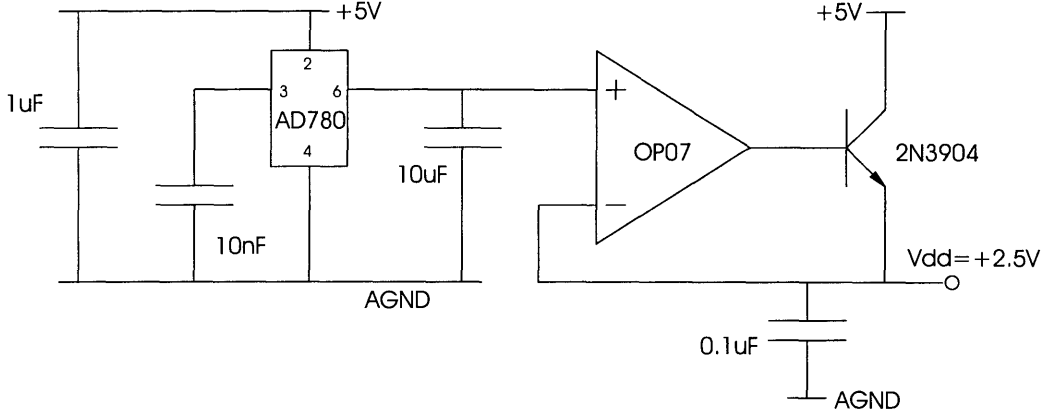


Figure 6-4: Vdd supply generation on analog test board

Our prototype chip requires approximately 42mA for static biasing. This translates into a static power consumption of 210mW. Almost all the bias current flows from the analog V_{dd} to the analog V_{ss} .

Current Biases

Current biases are used instead of voltage biases because currents can propagate along long traces without suffering from noise coupling from the substrate.

The two functional blocks, although sharing the same analog supplies, can be powered on and off independently. The on-board current biases generate two currents which are then connected to 2 different NMOS current mirrors on chip. In turn, they generate the necessary currents for the biasing of the opamps making up the C-V front-end and the modulator. Powering off a functional block is achieved by shorting the current input of the NMOS mirror to the negative supply, resulting in a zero gate-source voltage such that no current is supplied to the opamps within that functional block.

Implementation of the current bias is shown in figure 6-6. In essence, the opamp feedback action keeps the voltage across the 3.9k resistor constant such that a constant

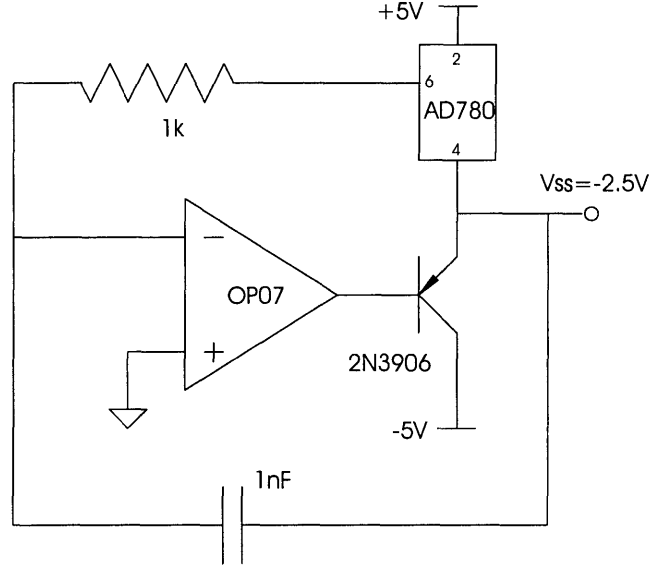


Figure 6-5: Vss supply generation on analog test board

current source I_{bias} is generated.

Clock Generation Circuitry

Six external clock signals are required for the chip to function. The two main clock signals ϕ_1 and ϕ_2 are for the functioning of the modulator and the C-V circuitry. Another two clocks ϕ_{chop1} and ϕ_{chop2} drive the choppers. Finally two clocks ϕ_{cm1} and ϕ_{cm2} drive the common mode feedback circuitry. The relative timing of these clocks is shown in figure 6-8.

These clock signals were generated using 2 PALs (Programmable Array Logic) and then buffered to transform the TTL logic levels to CMOS levels that can be applied directly to the clock input pins.

Refer to figure 6-7 which shows the clock generation circuit schematic. A master clock from an HP pulse generator at approximately 33MHz was used. The first PAL generates and cycles the 64 state numbers of the state machine designed. The second

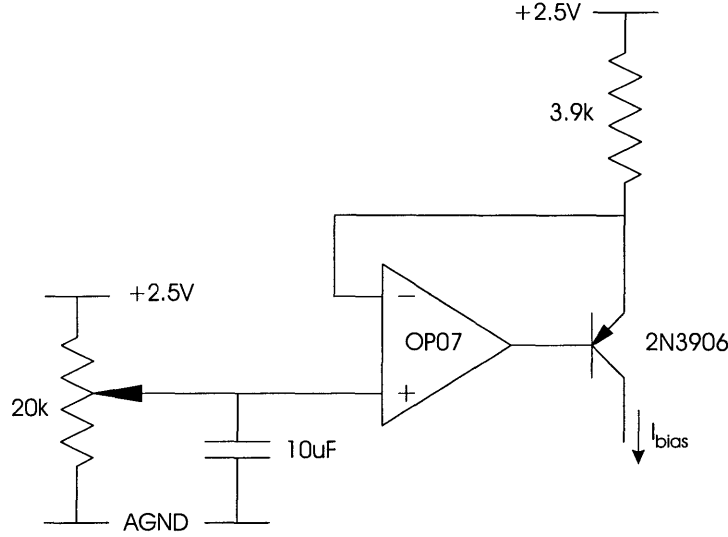


Figure 6-6: Bias current supply generation on analog test board

PAL decodes this state number giving rise to the appropriate clock signal transitions.

6.2.2 Bit-Stream Capture Scheme

A signal ACQ is also generated by the clock generation circuitry. Its main purpose is to offer a clock edge to synchronize the sampling of the modulator bit stream output mod_{5out} when mod_{5out} reaches a valid state. The signal ACQ is in essence ϕ_2 shifted by a quarter of a period such that ACQ has a positive transition at a quarter of a period later than ϕ_2 . This is shown in figure 6-9.

By design, the modulator bit-stream output mod_{5out} is only valid when ϕ_2 is active. When ϕ_2 is inactive, mod_{5out} is not guaranteed to assume any meaningful value. The scheme here aims at sampling mod_{5out} such that the final value it assumes during each active ϕ_2 is captured.

The sampling is performed using a Tektronix TDS420A digital oscilloscope. The oscilloscope has an external clock input clk_{ext} such that sampling of its input channels takes place when clk_{ext} has a high-to-low transition. The memory depth of each

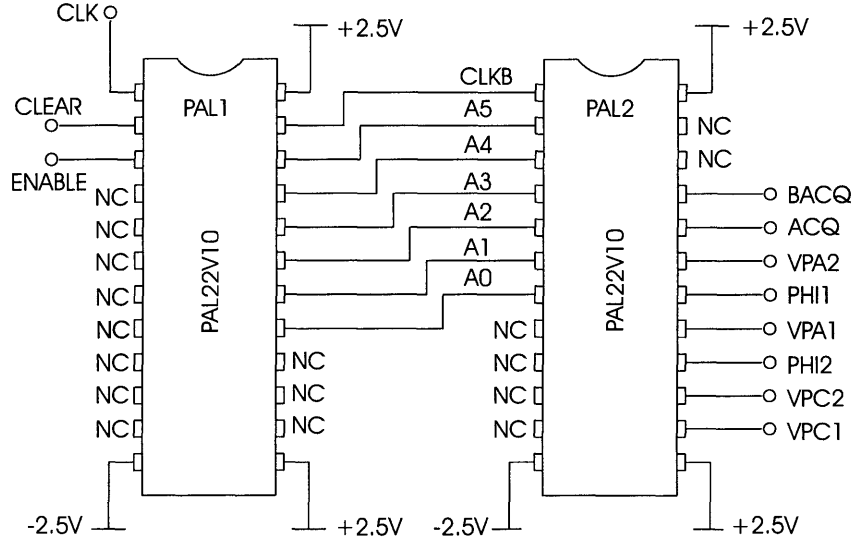


Figure 6-7: PAL connection for clock generation

channel is 120k data points. As a result, for a 1MHz master clock frequency the frequency resolution is on the order of 10Hz using 1 single channel. By using a 4-bit shift register clocked by *ACQ*, 4 times as many data points can also be collected.

After the data is captured in the oscilloscope memory, it is transferred to a text file on a floppy disk. This data is then read into MATLAB and signal processing is performed to calculate the power spectral density (PSD) and signal-to-noise ratio similar to that described in section 6.1.2.

6.2.3 Capacitance-to-Voltage Conversion Circuitry

One of the difficulties with the prototype testing lies with obtaining a pair of variable capacitors with known values. A compromise solution using two trimmer capacitors was implemented as shown in figures 1-3 and 6-12. On the test board the bases of a pair of glass trimmers were soldered onto a ground plane. The other ends were soldered directly to the 2 input pins of the C-V front-end. The values of the trimmers can then be set independently. However, the exact absolute values of the trimmers

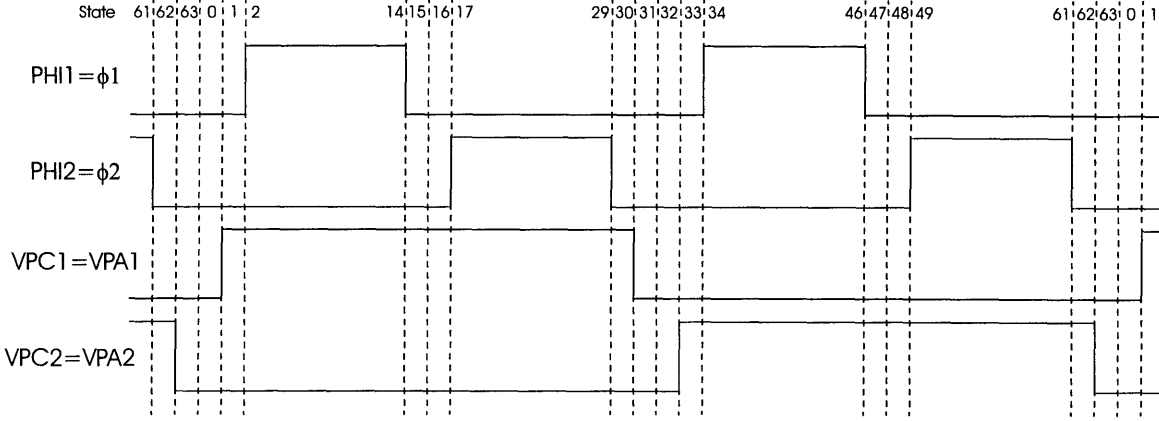
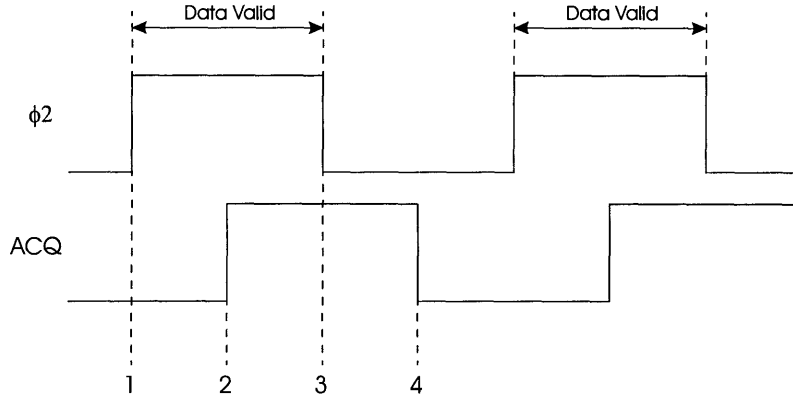


Figure 6-8: Relative clock phases

Figure 6-9: Acquisition clock (ACQ) relative to ϕ_2

are not known with accuracy.

Figure 6-10 shows the measured time-domain C-V front-end differential output voltages. The trimmers were set to a fixed value. The waveforms shown are similar to that obtained from HSPICE simulation.

By varying the settings on the trimmers, the differential C-V front-end output voltages were measured. Figure 6-11 plots the relationship between the differential output voltage magnitude and the trimmer settings. Here one trimmer was fixed while the other was adjusted in quarter turn increments and decrements. These increments

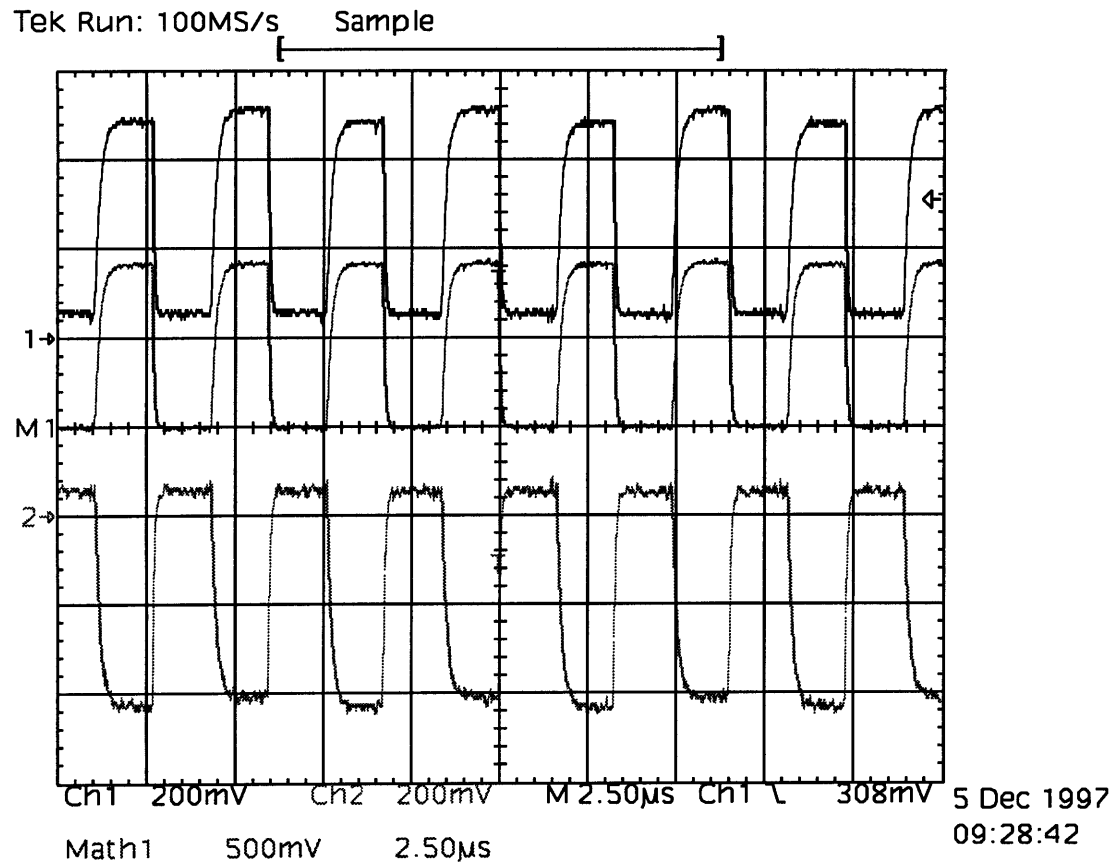


Figure 6-10: Measured transient voltage output from C-V front-end

corresponds to approximately increasing and decreasing the differential capacitance by $\frac{1}{4}$ pF. However the relationship between the turns and capacitances is not exact, owing to the limitations of the mechanics of the trimmer. Consequently figure 6-11 serves only as a functionality demonstration rather than a calibration.

6.2.4 5th Order Modulator

Figures 6-13 show the PSD from the actual measured data from our prototype chip. The input signal is a 2-V 500Hz differential sinusoid coming from an audio generator. This signal appears as a spike in the PSD plots. In addition, the high frequency noise

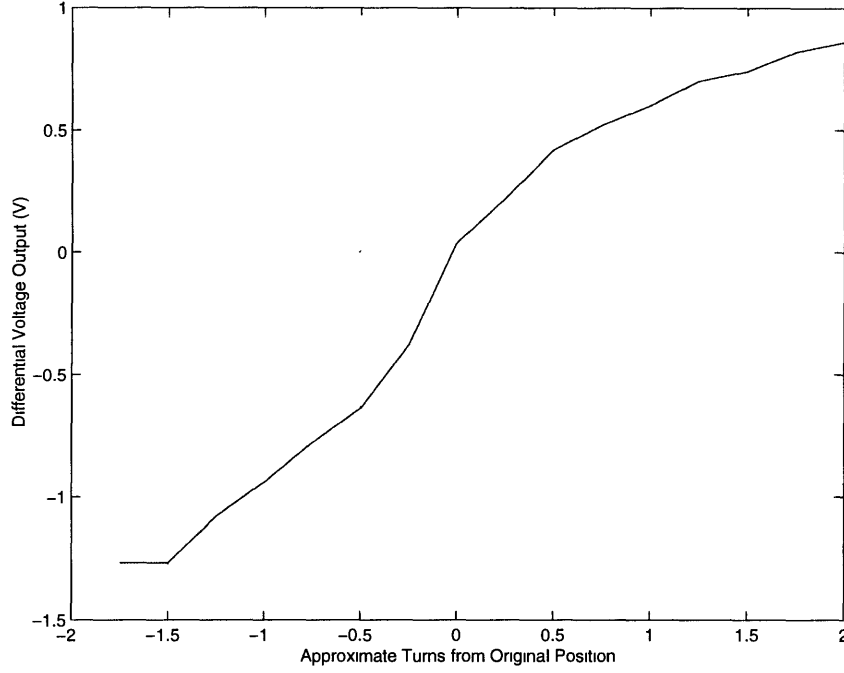


Figure 6-11: Plot of differential voltage output from C-V front-end against trimmer capacitor settings

shaping characteristics of the modulator is evident and comparable with simulation results.

The low frequency portion of the spectrum shows a higher-than-expected noise floor. It was found that part of the problem is due to the complementary clock generation. Please refer to figure 5-7 which shows the last integrator of the modulator, the comparator, and the differential feedback scheme. Essentially the feedback capacitors start to discharge onto the input nodes of the opamp once ϕ_2 goes high. However, the clock signal $\overline{\phi_2}$, being generated on-chip through an inverter, has an inverter delay of a few nano-seconds compared to ϕ_2 . Hence the comparator may not yet resolve, i.e., its outputs X and \overline{X} can assume an intermediate voltage near the middle of the supplies, thus setting off the wrong discharging of the feedback capacitors on the rising clock edge of ϕ_2 . This results in a rise in the ‘noise floor’ of the modulator as

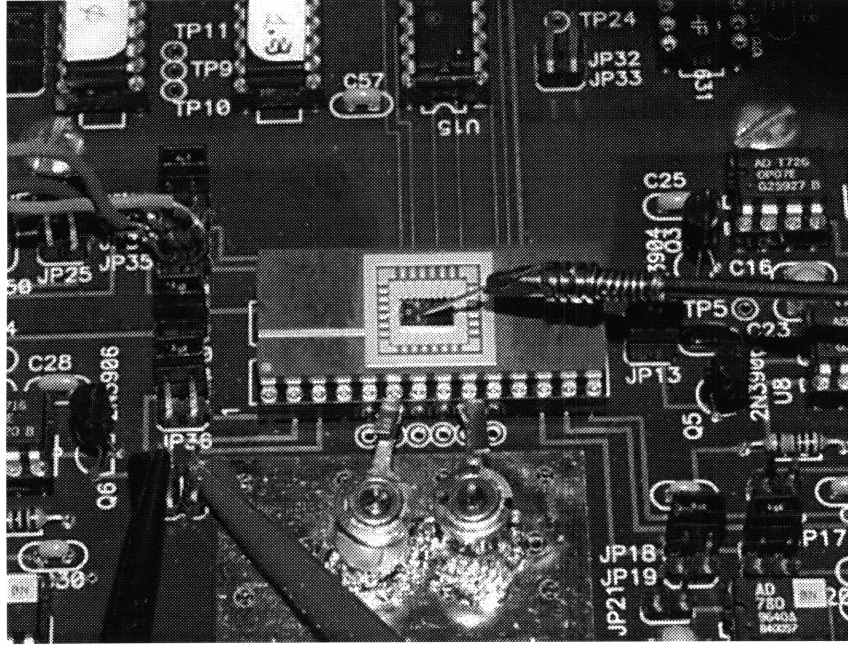


Figure 6-12: The test setup, showing an external probe feeding the clock signal $\overline{\phi_2}$ and the two trimmer capacitors

seen in figure 6-13.

This problem was fixed by laser-cutting two traces on the die itself, thus isolating the inverter which drives the on-chip clock signal $\overline{\phi_2}$ from the external clock ϕ_2 . The clock signal $\overline{\phi_2}$ was then supplied via a probe through a probe pad on the chip. Thus, this clock delay problem was largely eliminated. Figure 6-12 shows the probe which feeds the external clock signal onto the die.

Figure 6-14 shows the modulator spectrum using the externally-driven $\overline{\phi_2}$ clock. The fix was originally suggested by HSPICE simulations of the extracted layout and the measured results confirmed the suggestion. The noise floor was lowered by approximately 40dB yielding a converter resolution of 10 bits.

A few reasons can account for the measured results. One of them is the switched-capacitor $\frac{kT}{C}$ noise associated with the first integrator of the modulator, together with the lack of a reset mechanism for the comparator implementation. However the main

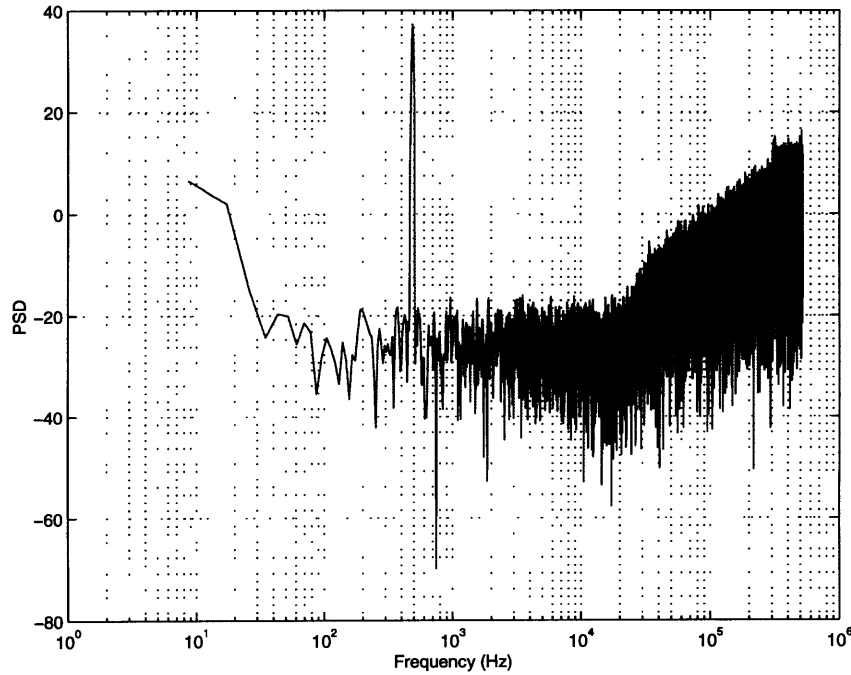


Figure 6-13: Measured modulator spectrum, with input being sinusoidal signal at 500Hz, 2.0V peak-to-peak, 120k data points

reason lies with the design rule violation with the die layout.

The sampling and feedback capacitors of the first stage of the modulator were sized to be 0.5pF. These were found to be too small from $\frac{kT}{C}$ noise considerations. The wide-band $\frac{kT}{C}$ noise associated with these capacitors is indistinguishable from the input signal itself and hence a white noise floor results. Theoretical calculations show that the total $\frac{kT}{C}$ noise contributed by these capacitors limits the modulator signal-to-noise ratio to 100dB after decimation and digital low-pass filtering. In order to achieve a resolution of 20-bit these capacitors should be sized as 8.2pF each such that the total noise contribution from these capacitors is at 120dB below the input signal level.

The design does not include a reset mechanism for the comparator. During the sampling phase of the integrator, i.e. ϕ_1 , the 5th integrator has its outputs connected

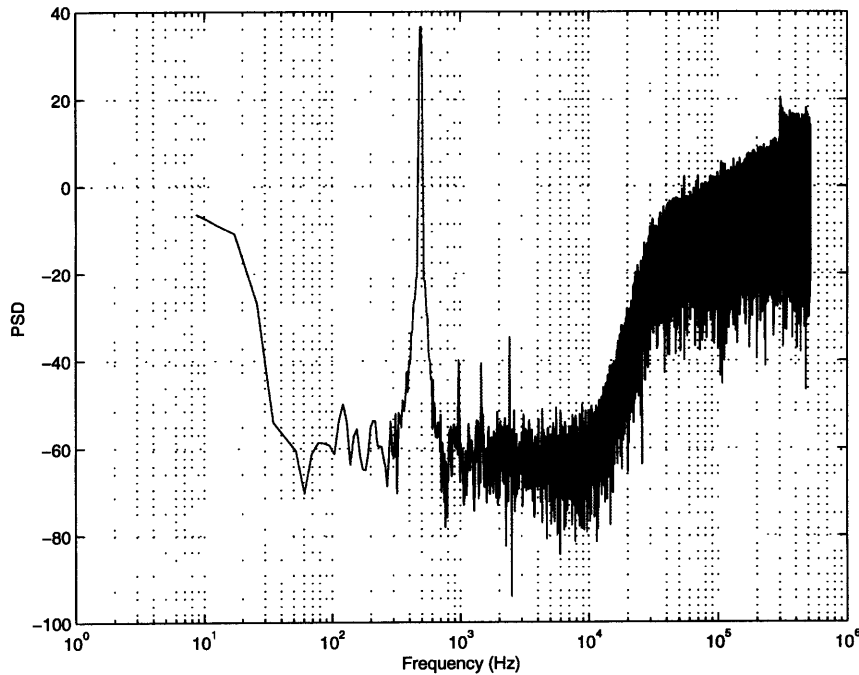


Figure 6-14: Improved measured modulator spectrum, with input being sinusoidal signal at 500Hz, 2.0V peak-to-peak, 120k data points

to the comparator inputs via CMOS pass gates. The idea is that the integrator can setup voltages at the comparator inputs such that they are the same as the integrator outputs. Being a differential design based on a pair of cross-coupled inverters, the comparator has its inputs at one of the digital supply voltages at the beginning of ϕ_1 . The resulting differential charge causes comparator hysteresis such that decisions are dependent on previous decisions, putting memory into the comparator. By numerical simulations, this was found to alter the high frequency characteristics of the modulator through the creation of unwanted system poles.

The main reason for the noise floor is the design rule violation of the CIF file submitted to MOSIS for fabrication. The scripts to translate the design from CA-DENCE to CIF introduced bugs in the layout design which were not caught until recently. Hence certain metal lines are shorted together on the chip itself as the

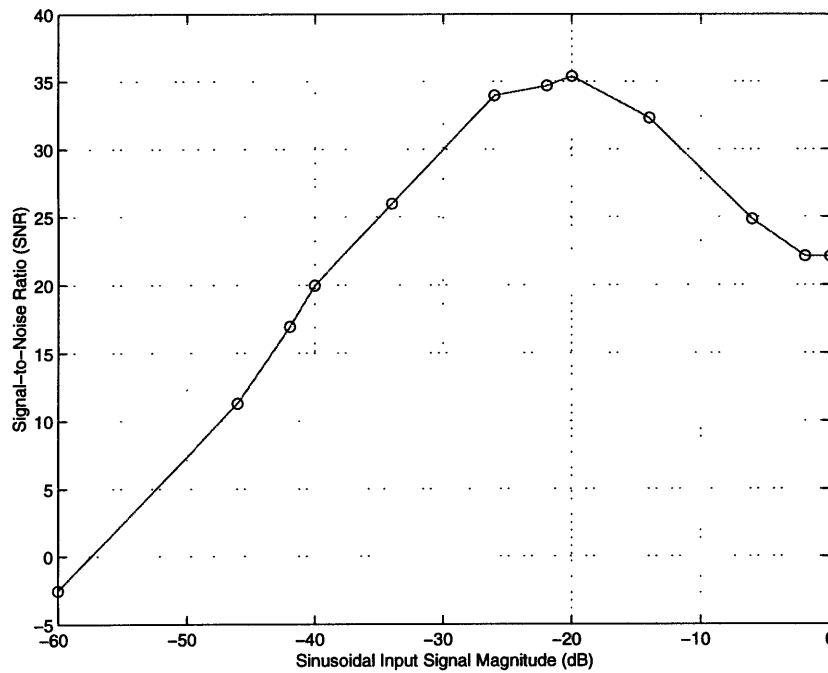


Figure 6-15: Signal-to-noise ratio plot for a 500Hz input signal, 120k data points

minimum clearance requirements are not met. Figure 6-15 shows the signal-to-noise ratio (SNR) plot for one particular test chip. The SNR obtained for a particular input signal varies from chip to chip because the extend to which the metal lines are shorted together is different for different test chips. As a result, different noise floor characteristics observed, and hence different SNR. For example, the SNR for the test chip shown in figure 6-15 is 22.1dB for a 1V magnitude, 500Hz sinusoidal input signal while that for another test chip is 44.9dB.

In summary, we have demonstrated the functionality of the two functional blocks, the capacitance-to-voltage conversion circuitry and the sigma-delta modulator, of our prototype chip. Further work has to be done to calibrate the C-V conversion circuitry. The performance of the sigma-delta modulator, however, is limited by design oversights and CIF file errors which will be addressed in the second-pass design.

Chapter 7

Conclusions

Throughout the course of any research, certain insights come to light that can significantly affect the documented results. Ideally, all this knowledge is obtained early enough so that the optimal theory may be developed and verified fully by the end of the study. However, important ideas surface continually and built upon the other ideas which has previously surfaced. No clear cutoff exists after which only testing and documentation should take place. Thus, when a period of research has ended, some realizations are fully solidified and others are just beginning to form. Any or all of this information may be applicable to future research. Hence these realizations are summarized and ideas for future research are presented in this chapter.

7.1 Conclusions

The implementation is a demonstration of the feasibility of constructing a capacitive displacement measurement system using a custom integrated circuit based solution. A main advantage over the current discrete implementations is the ability to locate the sensor electronics in close proximity to the sense electrode such that the triaxial

cable and its associated connections can be eliminated. The sensor chip converts the capacitance caused by displacement changes to a digital representation of the corresponding displacement. This digital output can then be captured for storage and analysis.

One drawback of the switched-capacitor based implementation employed is that the sense capacitance is charged such that the voltage across it is constant. It is more desirable to alter the scheme such that a constant charge is stored every time it is charge. A possible topology for achieving this is presented in section 7.2.2.

The prototype chip implemented is an important first step towards achieving the targets laid out at the beginning of this thesis. We have demonstrated basic functionality of the concept of integrating a switched-capacitor based sigma-delta modulator with the capacitive-to-voltage conversion circuitry on the same die. It was found that testing, characterization and calibration of our prototype chip was largely limited by our ability to locate a good calibrated variable differential capacitor with known precision.

7.2 Suggestions for Future Directions

There are two possible paths for further research. One is the modification of our current prototype implementation to incorporate the capacitance-to-voltage conversion circuitry into the sigma-delta modulator. Another one is a completely different approach which involves using an ac current as the excitation signal for the displacement probe.

7.2.1 Integration of C-V Circuit into Modulator Design

The highest performance system can be achieved if we can minimize the number of potential noise sources. Here, by incorporation of the C-V circuitry into the modulator design, i.e., using the probe capacitance as the input sampling capacitors in the modulator, the C-V circuitry essentially becomes the first integrator stage of the modulator, thus minimizing potential noise sources.

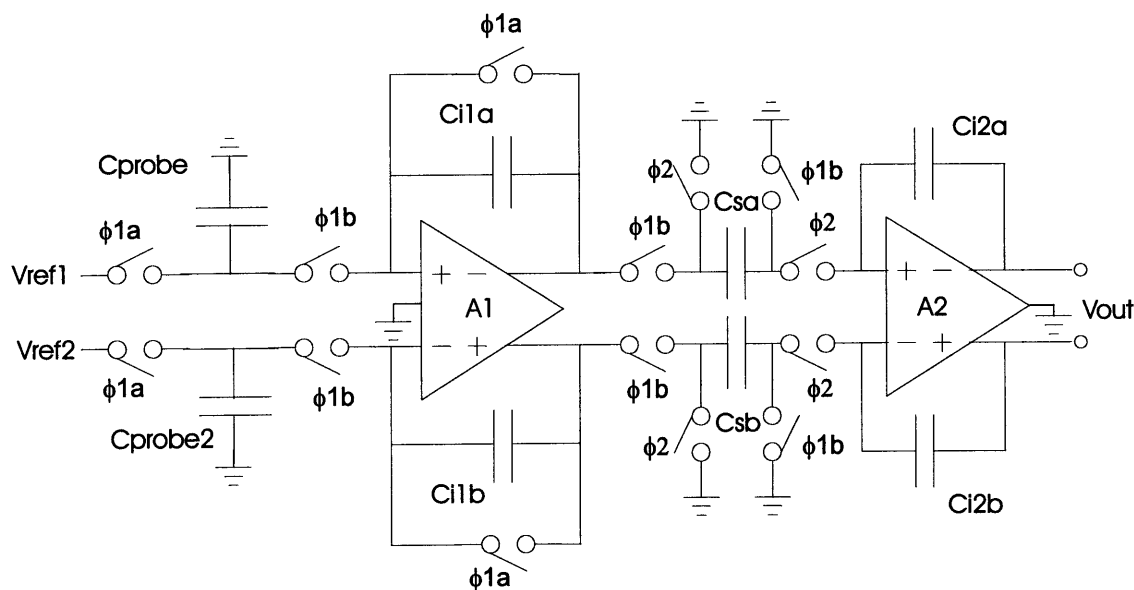


Figure 7-1: Possible first integrator of new modulator design

Figure 7-1 shows the proposed implementation of the first integrator of the modulator. Opamp A1 is an amplifier which has input common mode feedback while A2 is one that has output common mode feedback. Opamp A1, together with the associated capacitors C_{i1a} and C_{i1b} , implements the c_1 coefficients of the modulator as well as the capacitance-to-voltage conversion. Amplifier A2 acts as the integrator that also eliminates the potential large common mode voltage at the outputs of amplifier A1. Clocking of the switches are arranged such that a direct replacement of first integrator of the original modulator as shown in figure 5-2 is feasible, with the

addition of appropriate feedback capacitors connected to the opamp inputs of opamp A1 to implement the b_1 coefficient.

Figure 7-1 also shows the use of two voltage references V_{ref1} and V_{ref2} instead of a single reference as in figure 5-1. One possibility is to use this sensor chip in a feedback configuration such that one of the references V_{ref1} is adjusted until the chip output becomes zero. If such a condition is reached, the charges on C_{probe} and C_{probe2} are matched. Now the voltage of V_{ref1} is inversely proportional to C_{probe} and directly proportional to the displacement of interest.

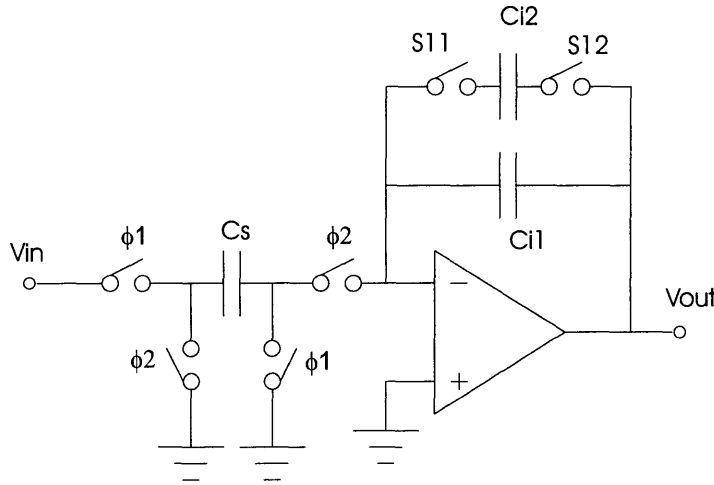


Figure 7-2: Altering the integrator gain

To counter the effects of large unknown parasitic capacitances connected in parallel with the sense capacitance on the optimal sizing for the integrating capacitors for the first integrator, an array of same-size on-chip capacitors can be used to form the feedback and integrating capacitors of the first integrator. Figure 7-2 shows a simple single-ended switched-capacitor integrator illustrating this concept. Essentially an extra capacitor C_{i2} can be switched in or out, thus altering the desired signal transfer function $\frac{V_{out}}{V_{in}}$ of the integrator from $\frac{C_s}{C_{i1}} \frac{z^{-1}}{1-z^{-1}}$ to $\frac{C_s}{C_{i1}+C_{i2}} \frac{z^{-1}}{1-z^{-1}}$. If C_{i2} is sized to be the same as C_{i1} , closing of the switches $S11$ and $S12$ essentially maintains the same

transfer function but halves the gain. Using this concept at the input stage of the modulator, we can adjust the input range of the modulator and consequently be able to counter the effects of having large unknown parasitic capacitors in parallel with the sense capacitance without the pessimistic scaling of on-chip capacitors.

7.2.2 On-chip Constant Current Drive Circuitry

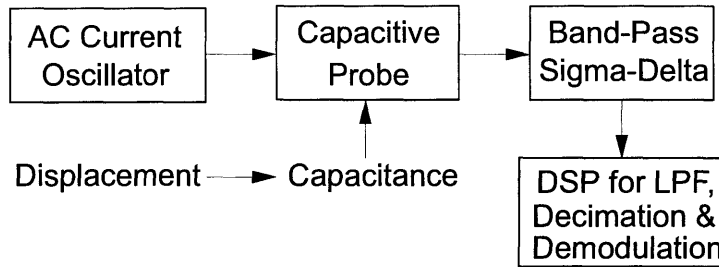


Figure 7-3: Possible integrated circuit compatible constant current probe

A constant-current drive topology essentially tries to maintain the charge on the sense capacitor constant such that the voltage developed across it is inversely proportional to the capacitance to be measured. The topology proposed here, as shown in figure 7-3, is to use an ac current generated by a log-domain based current oscillator [63, 64] as the drive signal for the sense capacitance. The resulting ac voltage developed across the sense capacitance is then buffered and converted by a band-pass sigma-delta modulator to a digital representation. Demodulation is then used to obtain the voltage that represents the capacitance to be measured and thus the corresponding displacement.

The use of a current as the excitation signal to the capacitive displacement probe is an advantage and also a challenge. One difficulty is the dc component coming from the current oscillator, as it will charge up the sense capacitance. A possible solution can be the use of a low-pass filter on the resulting voltage developed across the sense

capacitance. This filtered voltage signal is then compared to the desired operating point, for instance the analog ground voltage, and the difference is used to adjust the biasing of the output stage of the current oscillator such that this difference is minimized.

In short, we have demonstrated the feasibility of the integrated capacitive displacement sensor concept using an integrated circuit approach. Further research and investigation needs to be done in this promising area, especially regarding the integration of the capacitance-to-voltage conversion circuitry into the analog-to-digital conversion circuitry, as well as the constant-current drive circuitry.

Bibliography

- [1] Abbe et al. Capacitive thickness gauging for underground elements. U.S. Patent Office, Patent # 3 990 005, Nov 1976.
- [2] Abbe et al. Wafer flatness station. U.S. Patent Office, Patent # 4 860 229, Aug 1988.
- [3] Mallory et al. Wafer testing and self-calibration system. U.S. Patent Office, Patent # 5 642 298, Jun 1997.
- [4] M. L. Holmes. *Analysis and Design of a Magnetically-Suspended Precision Motion Control Stage*. M.S. Thesis, UNC Charlotte, 1994.
- [5] M. Ashburn. *A High Precision Fully Integrated Accelerometer*. S.M. Thesis, M.I.T., 1995.
- [6] M. Lemkin & B. Boser. A micromachined fully differential lateral accelerometer. In *CICC Dig. Tech. Papers, IEEE Custom Integrated Circuits Conference*, May 1996.
- [7] Analog Devices. $\pm 1g$ to $\pm 5g$ single chip accelerometer with signal conditioning. ADXL05 Data Sheet, 1995.

- [8] L. Zimmermann et. al. Airbag application: a microsystem including a silicon capacitive accelerometer, cmos switched capacitor electronics and true self-test capability. *Sensors and Actuators A*, 46–47:190–195, 1995.
- [9] O. Krömer et. al. High-precision readout circuit for liga acceleration sensors. *Sensors and Actuators A*, 46–47:196–200, 1995.
- [10] B. Boser & D. Auslander M. Lemkin. A fully differential lateral $\Sigma\Delta$ accelerometer with drift cancellation circuitry. In *Proceedings for IEEE Solid-State Sensor and Actuator Workshop*, Jun 1996.
- [11] T. Nagata et. al. Digital compensated capacitive pressure sensor using cmos technology for low pressure measurements. In *TRANSDUCERS '91 Digest of Technical Papers*, pages 308–11, Jun 1991.
- [12] J.A. Lloyd. *An Integrated Circuit Pressure Sensing System with Adaptive Linearity Calibration*. Ph.D. Thesis, M.I.T., 1997.
- [13] J. Bryzek. Impact of mems technology on society. *Sensors and Actuators A*, 56:1–9, 1996.
- [14] Ludwick et al. Modeling and control of a six degree-of-freedom magnetic/fudidic motion control stage. *IEEE Transactions on Control Systems Technology*, 4(5):553–564, Sep 1996.
- [15] C. Cornila et al. Capacitive sensors in cmos technology with polymer coating. *Sensors and Actuators B*, 24–25:357–361, 1995.
- [16] T. Kuroiwa et. al. A thin-film polysulfone-based capacitive-type relative-humidity sensor. *Sensors and Actuators B*, 24–25:692–695, 1995.

- [17] M. Lemkin & B.E. Boser C. Lu. A monolithic surface micromachined accelerometer with digital output. *IEEE Journal of Solid-State Circuits*, 30(12):1367–1373, Dec 1995.
- [18] ADE Corporation. Non-contact dimensional gaging using capacitive sensing. Presented at Sensors Expo, 1987.
- [19] P.T. Flowers. Capacitive position sensor. U.S. Patent Office, Patent # 4 694 235, Sep 1987.
- [20] A. Miller. Variable capacitance transducer. U.S. Patent Office, Patent # 3 517 282, June 1970.
- [21] K.B. Klaassen & K.C.L. Van Peppen. Linear capacitive microdisplacement transduction using phase readout. *Sensors and Actuators*, 3:209–220, 1982.
- [22] A. Fertner & A. Sjölund. Analysis of the performance of the capacitive displacement transducer. *IEEE Transactions on Instrumentation and Measurement*, 38(4):870–875, Aug 1989.
- [23] S. J. Ludwick & D. L. Trumper. Noise optimal control of a fluid floated magnetic positioner. In *Proceedings of the 1996 ASME International Mechanical Engineering Congress and Exposition*, volume DSC-58, pages 309–316, Atlanta, GA, Nov 1996.
- [24] Benadda et. al. A measuring device for the determination of the electrical permittivity in the frequency range 0.1–300 mhz. *J. Phys. E: Sci. Instrum.*, 15:132–136, 1982.
- [25] Y. Matsumoto & M. Esashi. An integrated capacitive absolute pressure sensor. *Electronics & Communications in Japan, Part 2*, 76(1):451–461, 1993.

- [26] Y. Matsumoto & M. Esashi. Integrated silicon capacitive accelerometer with pll servo technique. *Sensors and Actuators A*, 39:209–217, 1993.
- [27] Abbe et al. Self inverting gauging system. U.S. Patent Office, Patent # 4 217 542, Aug 1980.
- [28] Abbe et al. Self inverting gauging system. U.S. Patent Office, Patent # 4 353 029, Oct 1982.
- [29] S.M. Huang et al. Electronic transducers for industrial measurement of low value capacitances. *J. Phys. E: Sci. Instrum.*, 21:242–250, 1988.
- [30] A.S. Nizamani. Duty cycle based digital capacitance meter. *Int. J. Electronics*, 74(3):411–421, 1993.
- [31] C.A. Leme & H. Baltes T. Boltshauser. High sensitivity cmos humidity sensors with on-chip absolute capacitance measurement system. *Sensors and Actuators B*, 15–16:75–80, 1993.
- [32] M. Esashi & D. Uehara. Fabrication of a monolithic capacitance pressure sensor for gauge pressure measurement. *Electronics & Communications in Japan, Part 2*, 76(7):85–91, 1993.
- [33] A. Cichocki & R. Unbehauen. Application of switched-capacitor self-oscillating circuits to the conversion of rlc parameters into a frequency or digital signal. *Sensors and Actuators A*, 24:129–137, 1990.
- [34] B. Marlow et. al. Measurement of very small capacitance changes in silicon capacitive sensors. In *Proceedings of MICRO 95*, pages 3–7, 1995.

- [35] H. Matsumoto & K. Watanabe. A switched-capacitor digital capacitance meter. *IEEE Transactions on Instrumentation and Measurement*, IM-35(4):555–559, 1986.
- [36] K. Kondo & W. Watanabe. A switched-capacitor capacitance measurement circuit with vernier scale. *IEICE Trans. Fundamentals*, E76-A(7):1139–1142, Jul 1993.
- [37] H. Shimizu & K. Watanabe H. Matsumoto. A switched-capacitor charge-balancing analog-to-digital converter and its application to capacitance measurement. *IEEE Transactions on Instrumentation and Measurement*, IM-36(4):873–878, Dec 1987.
- [38] J.T. Kung & H.S. Lee. A digital readout technique for capacitive sensor applications. *IEEE J. Solid-State Circuits*, 23(4):334–339, Aug 1988.
- [39] J.T. Kung & H.S. Lee. An integrated air-gap-capacitor pressure sensor and digital readout with sub-100 attofarad resolution. *Journal of Microelectromechanical Systems*, 1(3):121–128, Sep 1992.
- [40] D.R. McMahon. *A High Dynamic Range Capacitive Displacement Sensor*. M.S. Thesis, M.I.T., 1993.
- [41] J.K. Roberge. Method for the measurement of capacitance, with application to linear measurement of distance. U.S. Patent Office, Patent # 5 189 376, Feb 1993.
- [42] Poduje et al. A.c. capacitive gauging system. U.S. Patent Office, Patent # 4 918 376, Apr 1990.
- [43] N. Battersby & S. Porta C. Toumazou, editor. *Circuit and Systems Tutorials*, chapter 4. IEEE Press, New York, 1994.

- [44] R. Schreier & G. Temes S. Norsworthy, editor. *Delta-Sigma Data Converters*. IEEE Press, New York, 1997.
- [45] P. Steiner & W. Yang. A framework for analysis of high-order sigma-delta modulators. *IEEE Trans. Circuits Syst.*, 44(1):1–10, Jan 1997.
- [46] K. Shenoi B. Agrawal. Design methodology for sigma-delta modulators. *IEEE Transaction on Communications*, pages 360–369, Mar 1983.
- [47] W. Lee & C.G. Sodini K.C.H. Chao, S. Nadeem. A higher order topology for interpolative modulators for oversampling a/d converters. *IEEE Trans. Circuits Syst.*, 37:309–318, Mar 1990.
- [48] W. Bennett. Spectra of quantized signals. *Bell System Technical Journal*, 27:446–472, Jul 1948.
- [49] R.C. Luo. Sensor technologies and microsensor issues for mechatronics systems. *IEEE/ASME Transactions on Mechatronics*, 1(1):39–49, Mar 1996.
- [50] C.H. Giancarlo & C.G. Sodini J.W. Scott, W.L. Lee. Cmos implementation of an immediately adaptive delta modulator. *IEEE Journals of Solid-State Circuits*, SC-21(6):1088–1095, Dec 1986.
- [51] S. Nadeem. *A 16-Channel Oversampled Analog-to-Digital Converter For Multi-channel Applications*. Ph.D Thesis, M.I.T., 1993.
- [52] R.M. Gray. Oversampled sigma-delta modulation. *IEEE Trans. Comm.*, COM-35(5):481–489, May 1987.
- [53] R.M. Gray. Quantization noise spectra. *IEEE Trans. Information Theory*, IT-36:1220–1244, Nov 1990.

- [54] R. Adams et. al. Theory and practical implementation of a fifth-order sigma-delta a/d converter. *J. Audio Eng. Soc.*, 39(7/8):515–528, Jul/Aug 1991.
- [55] H.E. Hilton. A 10-mhz analog-to-digital converter with 110-db linearity. *Hwelett-Packard Journal*, pages 105–111, Oct 1993.
- [56] S. Setty & C. Toumazou. ± 1 v cmos rail to rail op amp. In *Proceedings of ISCAS '95*, pages 1540–1543, Jun 1995.
- [57] J. Lloyd & H.S. Lee. A cmos op amp with fully-differential gain-enhancement. *IEEE Trans. Circuit Syst. II*, 41(3):241–243, Mar 1994.
- [58] K.C. Hsieh et. al. A low-noise chopper-stabilized differential switched-capacitor filtering technique. *IEEE Journal of Solid-State Circuits*, SC-16(6):708–715, Dec 1981.
- [59] R. Gregorian & G.C. Temes. *Analog MOS Integrated Circuits for Signal Processing*. Wiley, 1986.
- [60] S. Nadeem. *Design And Implementation of Fourth Order Modulator For 16-Bit Oversampled A/D Converter*. M.S. Thesis, M.I.T., 1989.
- [61] R.T. Howe & C.G. Sodini. *Microelectronics - An Integrated Approach*. Prentice Hall, 1997.
- [62] T.E. Adams. *An Integrated Circuit Biosensor for Hyperthermia Cancer Treatment*. S.M. Thesis, M.I.T., 1996.
- [63] A. Thanachayanont et. al. State-space synthesis of oscillators based on the mosfet square law. *Electronics Letters*, 32(18):1638–9, Aug 1996.
- [64] A. Thanachayanont et. al. A current-mode phase-locked loop using a log-domain oscillator. In *Proceedings of ISCAS '97*, pages 277–280, Jun 1997.